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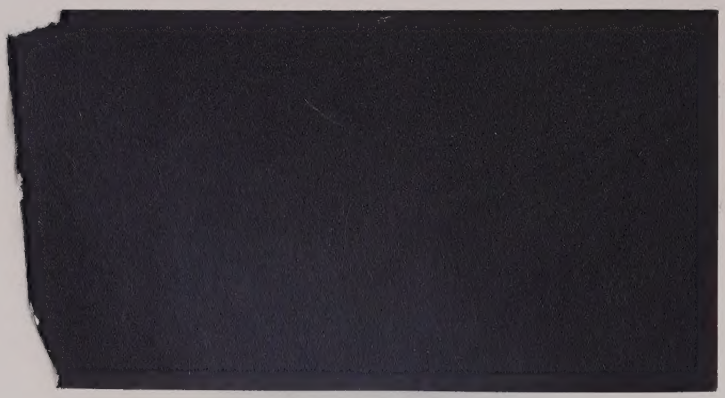
MODEL 153
STROBING VOLTMETER

E-H RESEARCH LABORATORIES, INC.
163 ADELINE STREET · OAKLAND, CALIFORNIA 94607



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STROBING VOLTMETER

Serial No. _____

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Units, abbreviations and prefixes of the International system of Units (SI) are used in this manual. Discrepancies may be noted between the terms used in the text and the instrument panel markings (e. g. ; hertz, kilohertz, megahertz for cps, kilocycles, megacycles, etc.).

The National Bureau of Standards announced its approval of the SI in February 1964, and subsequently the document was adopted by Congress as a national standard.

WARRANTY

E-H instruments are warranted to be free from defects in material and workmanship for one year. For in-warranty repair of this instrument, contact E-H Research Laboratories, Inc. , Customer Service Department and provide:

a. Instrument model number and serial number.
b. Details concerning the nature of the malfunction.

Shipping instructions, or repair information and parts will be sent to you promptly.

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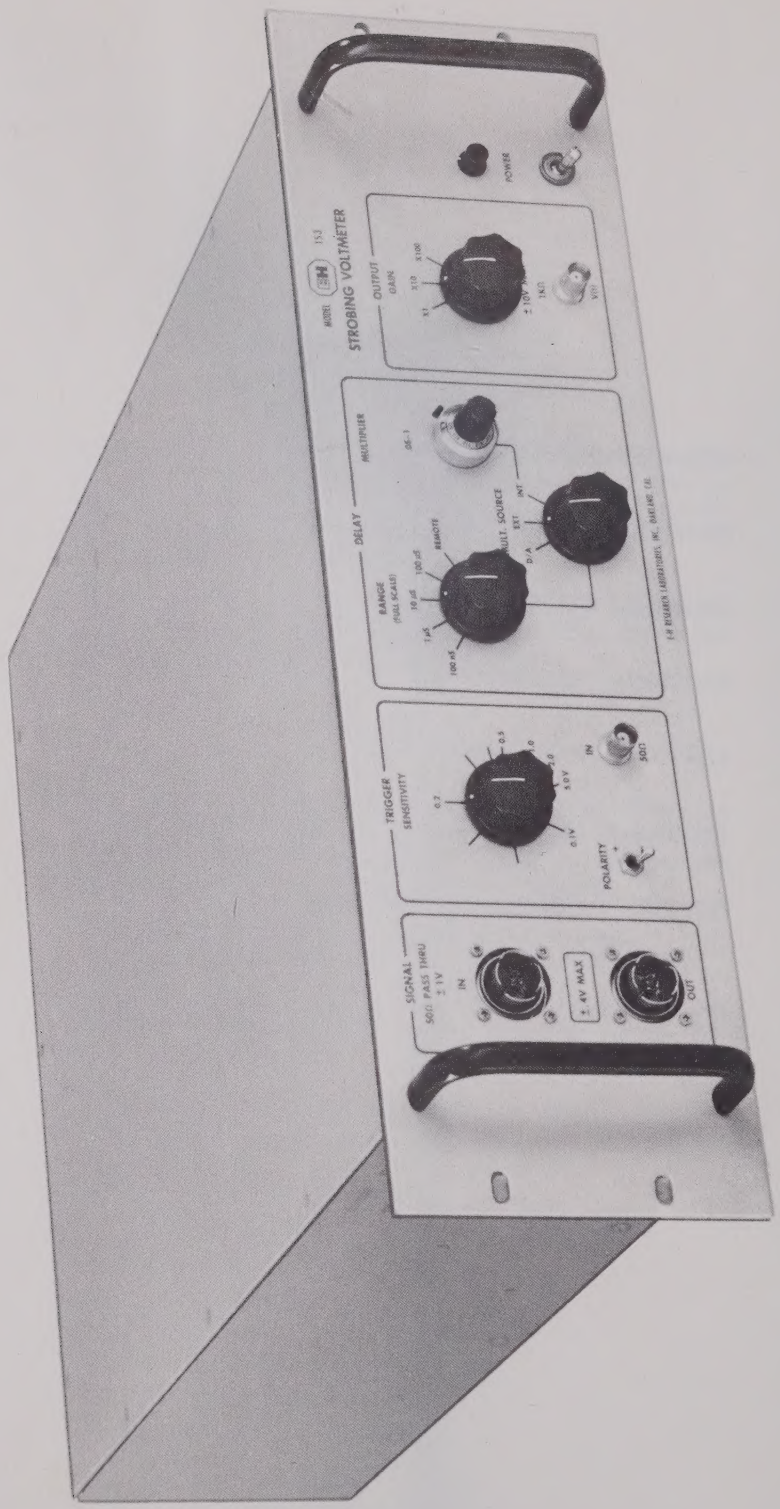


Fig 1-1 Model 153 Strobing Voltmeter

(A)

SECTION 1
SPECIFICATIONS

1-1 GENERAL

The E-H Model 153 is a versitile one-shot sample-and-hold strobing voltmeter capable of making instantanious voltage amplitude measurements on fast waveforms. The voltage-measurement point-in-time may be delayed from 5 ns to 105 μs following a measurement enabling trigger. Performance parameters may be determined by front-panel mounted controls, or programmed by externally applied logic and analogs.

1-2 SPECIFICATIONS

a. Signal Channel.

(1) Risetime. 3 ns, equivalent to more than 100 MHz bandwidth.

(2) Noise. 75 mv p-p, refered to the input, (p-p noise includes 95% distribution).

(3) Dynamic Range. ±1v combined dc and peak ac (refered to the dc offset voltage), ±4v max safe level.

(4) Voltage Accuracy. 2% + noise. In most cases, careful technique can yeild voltage amplitude measurements approaching 0.1%.

(5) Signal Input/output. 50Ω feedthrough signal path makes the input signal available at the SIGNAL OUT connector for use by other instrumentation, return to the device under test, or termination.

(6) Signal Delay Line. 40 ns delay in series with the SIGNAL IN connector permits a measurement effectively coincident with the trigger.

(7) DC Offset. ±1v externally applied analog into 100Ω input impedance. Signal is measured relative to the dc offset.

b. Output.

(1) Output Level. ±10v max, 1 kΩ source impedance.

(2) Voltage Gain. Selectable: X1, X10, or X100. The input signal voltage at strobe time is measured relative to the dc offset voltage. The difference is amplified X1, X10, or X100 and is present at the output connector when the data record trigger occurs.

(3) Holding Time. 250 ms time-constant.

c. Measurement Delay.

(1) Delay Ranges. 100 ns, 1 μs, 10 μs, and 100 μs full scale. Selectable by front-panel switch or external program lines (+3v keys).

(2) Delay Vernier. Panel-mounted switch selects:

(2a) Front-panel mounted, 10-turn calibrated control. Useable delay from 5% to 105% of selected delay range.

(2b) D/A Converter, converts 3-decade, 12-line BCD logic to 0 to +5v delay analog. D/A converter may accept inputs from externally applied BCD logic, or from internally-mounted BCD counter (153-1 option).

(2c) External, 0 to +5v delay analog produces 0 to 100% of selected delay range. Input impedance is 1 kΩ.

(3) Triggered Delay Advance. When the BCD counter and the D/A converter cards are installed, the delay interval may be advanced 1/1000th of the selected delay range per measurement, allowing coherent sampling (153-2 option).

(4) Slaving. The delay analog output of the Model 153 may be used to slave the delay analog input of another Model 153. The output of the second 153 may be used to drive a third 153, etc. Additional slaving configurations are available as optional extras. Contact your E-H Representative, or the factory for specific information.

(5) Delay Accuracy.

(5a) 100 ns range; 0.35% of full scale +1% of programmed delay.

(5b) 1, 10, and 100 μs ranges; 0.35% of full scale +2% of programmed delay.

Any single range may be calibrated to the accuracy stated for the 100 ns range. BCD programming adds 3% of programmed delay to the specifications. Accuracy specifications are qualified as follows: (a) valid between 10% and 100% of full scale delay range, (b) a fixed offset error exists between the trigger T zero and the delay range T zero up to 5 ns +3% of full scale maximum.

(6) Delay Jitter. 0.05% of full scale delay range.

d. Trigger Requirements.

(1) Trigger sensitivity. 100 mv, polarity selectable by panel-mounted switch. Trigger attenuator continuously variable to 50:1. Maximum trigger signal; 20v attenuated, 4v unattenuated.

(2) Trigger Holdoff. Measurement cycles will be initiated up to 1 per ms from trigger repetition rates up to 20 MHz.

e. Programming.

(1) Delay Ranges. 3 key lines, +3v on the respective key line will select the 1 μs, 10 μs, or the 100 μs delay range. If none of the keying lines are energized, the delay range is 100 ns. Input impedance

for each line is 3 kΩ.

(2) Vernier Delay Analog. 0 to +5v into 1 kΩ input impedance produces delay from 0 to 100% of selected delay range.

(3) Vernier Delay Digital (with D/A card installed). 3-decade BCD, 12 key lines. +3v into 5 kΩ impedance per line.

f. Other Outputs.

(1) Delay Analog Out. 0 to +10v proportional to vernier delay programmed. 1 kΩ source impedance.

(2) Data Record Trigger. Not less than 0.5 μs trigger pulse occurring approximately 4 μs after strobe time.

g. Power Requirements. 105/125 vac, 50/60 Hz, 100 volt-amps (230 vac operation available by changing transformer taps).

h. Dimensions. 5 1/4 x 19" panel, 18 3/4" deep (133 x 483 x 476 mm).

i. Weight. 25 lbs. (11.4 kg) net. Domestic shipping package, 35 lbs. (15.9 kg). Export shipping package, 50 lbs. (20.9 kg).

j. Accessories included. 50Ω termination, GR No. 874 W505; Programming connector, Amphenol No. 5730240.

SECTION 2
OPERATING INFORMATION

2-1 GENERAL

The Model 153 Strobing Voltmeter uses a balanced diode-bridge to isolate its measuring circuitry from its 50Ω feed-through signal line. The bridge is gated on during a 4 ns strobe period. The time location of the strobe is variable relative to the measurement enabling trigger by panel-mounted controls or by remote program inputs.

The voltage present on the signal line at the end of the strobe period is compared to a dc offset level, the difference is passed through a memory amplifier chain. The memory amplifier chain has a voltage gain of 10, and a memory time-constant of 250 ms. An additional output amplifier with a voltage gain of 10, and a 10X attenuator allow panel-selectable scale factors of X1, X10, and X100.

The measurement cycle time of the Model 153 is initiated by an externally applied trigger. Once the measurement cycle is initiated, the trigger recognition circuit is locked out for 1 ms. The Model 153 is a single-shot device which is capable of making 1000 measurements per second. The fixed trigger lockout period allows time for auxillary equipment to accept the measurement information supplied by the Model 153 (data rates to 100 kHz are optional).

2-2 FUNCTION OF FRONT PANEL CONTROLS AND CONNECTORS

a. SIGNAL IN and SIGNAL OUT Connectors. A 50Ω loop-through signal line for the input signal to be measured. There is 40 ns of delay between the SIGNAL IN connector and the measurement bridge.

b. TRIGGER SENSITIVITY. Controls a balanced attenuator between the TRIGGER IN connector and the trigger discriminator. Permits triggering on signals from 100 mv to 20v.

c. TRIGGER POLARITY Switch. Controls the input connections to the trigger discriminator. Permits triggering on either positive or negative tirgger signals.

d. TRIGGER IN Connector. A 50Ω input for the measurement-enabling trigger signal.

e. DELAY RANGE Switch. A 5-position switch which selects either the 100 ns, 1 μs, 10 μs, 100 μs delay range, or selects remote programming for the delay range.

f. DELAY MULT. SOURCE Switch. Selects the source of the dc analog voltage to be used as the vernier delay multiplier. In the D/A position, the output from the D/A converter is used as the vernier delay multiplier. In the EXT position, the dc voltage applied to the rear-mounted DELAY ANALOG IN connector is used. In the INT position, the panel-mounted MULTIPLIER control determines the vernier delay multiplier.

g. DELAY MULTIPLIER. A 10-turn control which determines the vernier delay multiplier when the MULT. SOURCE switch is in the INT position. The control is continuously adjustable from 5% to 105% of the selected delay range.

h. OUTPUT GAIN Switch. Selects the overall voltage gain of the Model 153. The output voltage may be 1, 10, or 100 times the input voltage at strobe time, with the limitation that the output voltage is not more than + or - 10v.

i. V(t) Connector. The measurement output connector. The voltage present at this connector is proportional to the difference between the input signal and the dc offset voltage at strobe time. Source impedance is 1 kΩ, and the decay time-constant is 250 ms.

j. POWER Switch. Applies or disconnects primary power to all circuits in the Model 153. The associated pilot light indicates power on.

2-3 FUNCTION OF REAR PANEL CONNECTORS

a. J301. Primary power-line input, either 117 vac or 234 vac, 50/60 Hz, depending on the connections to the primary of the power transformer. See power supply schematic for 117/234 volt option.

b. J302. Remote programming connector. Provides connections to remote programming leads. See schematic section for pin connections.

c. DATA RECORD TRIGGER Output. A 0.5 μs trigger occurring approximately 4 μs after strobe time. The presence of a trigger at this connector indicates

that the measurement has been made, and an output is ready for use at the front panel-connector, V(t).

d. DELAY ANALOG OUT Connector. Provides an output voltage between 0 and +10v proportional to the vernier delay multiplier analog regardless of the source of the analog. Source impedance is 1 kΩ.

e. DELAY ANALOG IN Connector. Input connector for externally-applied vernier delay multiplier analog. When the front-panel DELAY MULT. SOURCE switch is in the EXT position, the voltage at this input connector determines the vernier delay multiplier factor. Input impedance is 1 kΩ, sensitivity is +5v for full scale delay on the selected delay range.

2-4 OPERATION

a. The waveforms which fall within the measurement capability of the Model 153 can contain appreciable frequency components in excess of 100 MHz. If any of these high-frequency components are attenuated through the use of connectors, cables, or attenuators that do not have a flat frequency response beyond 100 MHz, degradation of the waveforms will result. Mismatch effects can also degrade pulse waveforms; therefore, consideration and care must be taken to preserve the quality of signal and trigger waveforms when coupling to the system or device under test.

If the signal source-impedance of the device or system under test is other than 50Ω, use an impedance matching device so that mismatch effects will not degrade the waveform to be measured. Return the signal loop-through output connector to an effective 50Ω pure-resistive load. The signal loop-through output connector may be either terminated in 50Ω at the panel connector, or returned to a 50Ω environment.

Make sure that all connectors, attenuators, and cables are of proper impedance and have a flat frequency response in excess of 100 MHz. Use high-quality 50Ω coaxial cable, such as RG213/U. For best results, use short cables, since long cables tend to attenuate the high frequency components of fast waveforms. General Radio (GR) 874 series coaxial connectors are recommended for the signal path into and out of the Model 153.

b. Triggering. The measurement cycle of the Model 153 must be initiated by an externally applied trigger. The triggering signal initiates a 1 ms hold-off interval during which the trigger recognition circuit is locked out. Triggering signals may be applied with repitition rates up to 20 MHz. Triggering signals which occur during the 1 ms hold-off interval are not recognized. The trigger recognition circuit will accept the next trigger which agrees with the trigger polarity selector switch and the sensitivity control after the hold-off interval terminates.

Provisions are made in the trigger recognition circuit to prevent multiple triggering from a single wide triggering signal. The trigger signal must be at zero volts at the end of the hold-off interval, or revert to zero after the hold-off interval before a new cycle can be initiated.

The trigger input connector is internally terminated in 50Ω. The triggering signal should be from a 50Ω source, or impedance matched to the 50Ω trigger input. It should have a fast rise time, in the order of 1 ns, to avoid the uncertainty of where triggering occurs on the rise of the triggering waveform. The triggering signal should also have a finite jitter-free time relationship to the signal to be measured. These considerations are particularly important when making measurements on the 100 ns delay range.

The Model 153 has an effective T zero for each delay range. The effective T zero will be within 5 ns ±3% of the selected delay range from the time triggering occurs. Programmed delays are relative to this effective T zero. As long as the calibration of the instrument is not distrubed, the effective T zero for each individual range can be expected to remain fixed relative to the trigger.

c. Signal Handling. For reliable measurements the input signal to the Model 153 must be handled in accordance with good fast-pulse techniques. All cabling, connectors, and attenuators must be capable of transporting the signal to be measured through the signal loop-through path and to an effective 50Ω termination. The Model 153 will measure the voltage present at its sampling bridge at the end of the measurement strobe.

If the applied signal has been degraded or if reflections are present due to improper signal handling techniques, the measurement will be erroneous and misleading.

The signal handling portion of the Model 153 is confined to a 50Ω coaxial feedthrough loop which includes 27 ft. of RG214. This 40 ns of delay in the signal path allows time for switching in the trigger recognition and delay circuits. On the 100 ns delay range, with minimum delay programmed, it is possible to strobe in advance of a fast-rise signal which is time coincident with the trigger. When the Model 153 is used as a coherent sampler, this permits display of a leading edge which is coincident with the trigger.

For maximum bandpass capability, the delay cable may be removed. In this case, the effective delay interval will be 40 ns longer than the same programming would produce with the delay cable.

d. Delay Interval. The input signal voltage amplitude is sampled after a predetermined delay interval. The delay interval is initiated by the trigger and is continuously adjustable from 5 ns to 105 μs in four delay ranges. The delay interval may be determined by front-panel controls or by external programming.

To determine the delay interval, one of the four delay ranges must be selected and a dc analog must be provided. Full scale on the four delay ranges are: 100 ns, 1 μs, 10 μs, and 100 μs. The dc delay analog is a voltage from 0 to +5v corresponding to 0 to full scale on the selected delay range.

The desired delay range may be selected by the front-panel DELAY RANGE switch, or if the switch is in the REMOTE position, the delay range may be selected by applying +3v to the appropriate keying line in the rear-mounted programming connector, J302. There are three delay range keying lines, one each for the 100 μs, the 10 μs, and the 1 μs delay ranges. If none of these ranges are selected, the delay range is 100 ns full scale.

The selection of the source for the vernier delay analog voltage is independent of the selection of the delay range. The panel-mounted DELAY MULT. SOURCE switch selects INT, EXT, or D/A.

(1) When INT is selected, the panel-mounted DELAY MULTIPLIER provides the vernier delay voltage. The DELAY MULTIPLIER is continuously adjustable from 5% to 105% of the selected delay range.

(2) When EXT is selected, the voltage at the rear-mounted DELAY ANALOG IN connector provides the vernier delay analog voltage. The input impedance is 1 kΩ. The sensitivity at the DELAY ANALOG IN connector is +5v for full scale delay on the selected delay range.

The output from the DELAY ANALOG OUT connector is 0 to +10v from a 1 kΩ source impedance. When the DELAY ANALOG OUT from one Model 153 is connected to the DELAY ANALOG IN on another Model 153, the 1 kΩ source impedance and the 1 kΩ input impedance makes a 2:1 voltage divider. Thus the full scale output voltage matches the full scale input voltage, and one Model 153 can provide the DELAY ANALOG IN for another Model 153. The second Model 153 will be programmed for the same delay interval if both Model 153s have the same delay range selected.

The buffer amplifier in the Model 153 requires about 100 μs to slew to a new delay analog voltage. At least 100 μs should be allowed between the application of a new delay analog input and triggering of the measurement cycle.

(3) When D/A is selected, the output of the D/A converter card provides the vernier delay analog voltage. The D/A card permits digital programming of the delay analog voltage from an external source. In this mode of operation, the delay vernier is determined by the BCD logic on the 12 external programming lines. Each of the 12 key lines has 5 kΩ impedance. Logic 1 is +3v and logic 0 is 0v. The 12 key lines accept 3 decades of logic in a 1-2-4-8 BCD code, each bit representing 0.1% of the selected delay range.

The D/A card can also accept inputs from the internal BCD counter (if the counter card is installed). In this mode of operation, the counter is increased by one bit each time a measurement is made, permitting coherent sampling with 1000 dots/display density.

e. Output Data. The data output from the Model 153 is available at the front panel BNC connector labeled V(t). The output is a voltage waveform from a 1 kΩ source impedance. The output voltage rises to its peak value within 4 μs after strobe time and then decays with a 250 ms time-constant. The peak output voltage is between +10 and -10v, and is proportional to the difference between the input signal voltage amplitude and the dc offset voltage at strobe time. It is either 1, 10, or 100 times the measured input voltage depending on the position of the OUTPUT GAIN control on the front panel.

f. Coherent Sampling. With the digital counter card and the D/A converter card installed, the Model 153 may be used as a coherent sampler.

The digital counter card is a 3-decade BCD counter which increases count by 1 bit after each measurement strobe. The output of the digital counter is BCD logic on 12 keying lines which are connected to the D/A converter card and the rear-mounted programming connector, J302. Since the counter has 3-digit capacity, it delineates 1000 input bits.

The D/A card is a 3-decade digital-to-analog converter. The inputs to the D/A card are the 12 logic lines from the digital counter and/or the rear-mounted programming connector, J302. The D/A card converts the BCD logic on the 12 keying lines to an analog between 0 and +5v to be used as the vernier delay analog. Thus the selected delay range is divided into 1000 discrete steps, one of which is selected by the logic present on the BCD keying lines.

If the D/A card is driven from the counter card, the delay interval is increased by 1/1000 of the full scale delay range after each measurement strobe. Thus, 1000 successive triggers will scan from 0 delay to full scale of the selected delay range.

The waveform at the DELAY ANALOG OUT connector would be a 1000 increment stair step from 0 to +10v. The waveform at the V(t) output would be the voltage amplitude points on the input signal waveform that corresponds to each of the 1000 delay intervals.

The DELAY ANALOG OUT waveform can be used as the horizontal deflection voltage, and the V(t) output can be used as the vertical deflection voltage to produce a coherent sampling display on a relatively unsophisticated display device.

g. External Programming. The two functions that may be externally programmed are the delay range and the delay vernier. If the D/A converter board is installed, the delay vernier may be programmed either with 3-decade BCD logic or with a 0 to +5v analog.

The delay range is programmed by applying +3v to one of three delay range keying lines. There is one keying line each for the 1 μs, 10 μs, and 100 μs delay ranges. If all three of these keying lines are at 0v the 100 ns delay range is selected. The delay ranges are not mutually exclusive. Care must be taken not to program two or more ranges at the same time. For example, if +3v is applied simultaniously to the 100 μs and the 10 μs keying line, the effective delay range will be approximately 110 μs. The resulting measurement will probably be misleading. Refer to the schematic section of this manual for pin connections on the programming connector, J302.

The delay vernier may be externally programmed by applying a dc analog between 0 and +5v to the DELAY ANALOG IN connector, mounted on the rear plate. 0v corresponds to 0 delay, and +5v corresponds to full scale delay on the selected delay range. The voltage applied to the DELAY ANALOG IN connector may select delays from 0 to 105% of the selected delay range. Normally the programming should not select less than 10% of the selected delay range. If a delay of less than 10% of full scale is desired, the next faster range should be used.

If the D/A converter board is installed, the delay vernier may be externally programmed by applying 3-decade BCD logic to the 12 BCD keying lines. Refer to the schematic section of this manual for the specific pin connections in the programming connections in the programming connector, J302. The D/A converter board as normally supplied is non-latching, and accepts 3 decades of 1-2-4-8 BCD logic. Additional components may be added to the D/A converter board, or component values changed to accommodate a wide variety of logic. Consult your E-H Representative or the factory for specific information.

SECTION 3
THEORY OF OPERATION

3-1 GENERAL

This section of the manual contains an electrical description of each circuit in the Model 153 Strobing Voltmeter. A block diagram is included in the drawings section showing the overall relationship of the various circuits. Schematic circuit numbers are used to identify components in the circuit descriptions. Refer to the specific schematics in the drawings section to supplement the following discussion.

The 153 Strobing Voltmeter samples the instantaneous voltage amplitude of the signal applied to its 50Ω loop-through input. The time of sampling is delayed a predetermined interval after an externally-applied trigger. The delay interval may be set by front-panel controls, by externally applied programming, or the delay interval may be sequentially stepped by an internal counter.

3-2 BLOCK DIAGRAM

a. The measurement-enabling trigger is applied to a panel-mounted BNC connector. The input impedance is 50Ω. A panel-mounted sensitivity control permits adjusting the trigger sensitivity from 100 mv to 20v. A panel-mounted polarity-selector switch permits triggering on a positive trigger signal or a negative trigger signal.

b. The trigger discriminator amplifies the trigger signal and drives the trigger shaper.

c. The trigger shaper is a tunnel diode and a power amplifier. Providing the hold-off clamp has released from the previous measurement cycle, the trigger shaper switches the bistable multi.

d. The bistable multi is a fast-switching bistable multivibrator. It turns on the ramp gate, and is switched for the first 500 μsec of the 1000 μsec hold-off interval.

e. The ramp gate is a current commutating pair. In its quiescent condition it provides current to the hold-off switch. During the 500 μsec following triggering, when the bistable multi is switched, the ramp gate turns off the current normally supplied to the hold-off switch, and gates on the ramp generator.

f. The hold-off switch establishes the 1000 μsec hold-off interval. The hold-off interval is divided into two intervals of approximately 500 μsec each. All of the logic functions are performed during the first 500 μsec interval. The second 500 μsec interval permits the circuitry to return to its quiescent condition before being re-triggered.

The hold-off switch resets the bistable multi after the first 500 μsec of the hold-off interval. An output from the hold-off switch drives the hold-off clamp for the full 1 ms hold-off interval.

g. The hold-off clamp effectively shorts out the trigger shaper for the 1 ms hold-off interval. The applied trigger signal must revert to near zero after the hold-off interval has elapsed before the hold-off clamp will release the trigger shaper. Thus a trigger signal of more than 1 ms width can not initiate more than one measurement cycle.

h. The ramp generator, when gated on by the ramp gate, produces a linear delay ramp. The time duration of the delay ramp is determined by the ramp range selector. The output of the ramp generator provides an input to the ramp comparator, and also provides an input to the counter driver.

i. The ramp range selector determines the time duration (slope) of the delay ramp. The ramp range selector can be operated by a front-panel mounted control, or by external programming. If external programming is used, +3v on the proper keying line will select the 1 μs, 10 μs, or 100 μs range. If neither of these three ranges are selected, the delay ramp will be 100 ns.

j. The delay analog buffer accepts the 0 to +5v delay analog voltage. It provides an isolated output to the ramp comparator and to the DELAY ANALOG OUT jack. The delay analog buffer is a feedback stabalized amplifier with a voltage gain of 2 and an output impedance of 1 kΩ.

The input to the delay analog buffer is selectable by a front-panel control. The input can be from a panel-mounted 10 turn control, from the rear-mounted DELAY ANALOG IN jack, or from the internal D/A converter.

The 2X gain incorporated in the delay analog buffer

permits driving a 1 kΩ load from the 1 kΩ source impedance and achieving the same dc level across the load as at the input of the buffer amplifier. The alternative would be an amplifier with a gain of 1 and near zero output impedance. Such a low output impedance amplifier would not provide short circuit protection.

The delay analog output of the Model 153 will provide the delay analog input for another Model 153 directly, since the gain of 2 and the 1 kΩ output impedance is compatable with the 1 kΩ input impedance.

k. The ramp comparitor is a voltage-amplitude discriminator pair. The two inputs are the range ramp from the ramp generator, and a dc voltage level from the delay analog buffer. When the range ramp reaches amplitude-coincidence with the delay analog voltage, the ramp comparitor triggers the delayed pulse generator.

l. The delayed pulse generator is a one-shot multivibrator. It generates a 200 ns wide delayed pulse. The leading edge of the delayed pulse follows the measurement-enabling trigger by a time interval equal to the programmed delay. The leading edge of the delayed pulse triggers the strobe generator and the trailing edge triggers the memory gate generator.

m. The counter driver clamps the delay ramp at about 110% of full scale. After the full scale range interval has elapsed, the counter driver produces an output bit to increase the BCD counter by 1.

n. The BCD counter is a 3-decade counter. One bit is added from the counter driver after each range ramp is completed. The output of the BCD counter drives the D/A converter and/or the 12 external BCD logic lines.

o. The D/A converter is a digital-to-analog converter. It is either driven by the internal BCD counter or from external BCD programming. When the D/A converter is driven by the BCD counter, the output is a 1000 increment voltage stair-step from 0 to +5v. When the D/A converter is driven from the external programming lines, the output is an analog equivalent of the numerical value of the BCD logic. In either case, the output of the D/A converter is available as the delay analog voltage. It determines the vernier delay when the panel-mounted DELAY MULT. SOURCE switch is in the D/A position.

p. The strobe generator is triggered by the leading edge of the delayed pulse. The output of the strobe generator is a 4 ns strobe at the end of the delay interval. During the strobe pulse, the applied signal is connected through the sampling bridge to the first memory input.

q. The DC offset amplifier isolates the dc offset voltage source and biases the first memory amplifier. The signal to be measured is sampled relative to the dc offset voltage. The output of the Model 153 is proportional to the difference between the applied signal and the dc offset voltage

r. The first memory amplifier amplifies the signal sample by a factor of 4, and drives the second memory amplifier through the memory gate bridge.

s. The memory gate generator is triggered by the trailing edge of the delayed pulse. The output is a 1.2 μsec gate starting 200 ns after strobe time.

t. The memory gate bridge connects the output of the first memory amplifier to the input of the second memory amplifier for the duration of the 1.2 μsec memory gate.

u. The second memory amplifier further amplifies the signal sample by a factor of 2.5. The second memory has a long-decay time-constant, approximately 250 ms. Gain adjustments and dc level adjustments are made in the second memory amplifier. The voltage gain from the signal input to the output of the second memory amplifier is 10X.

v. The voltage gain of the output amplifier is selectable by a front-panel control. The output of the second memory amplifier may be attenuated by a factor of 10, connected directly to the output jack, or amplified by a factor of 10. This allows an overall voltage gain from the input of 1, 10, or 100. The output amplifier provides the output signal to the panel-mounted output jack, V(t).

w. The 3 μsec delay is triggered by the trailing edge of the memory gate. The 3 μsec delay starts 1.4 μsec after strobe time. The output of the 3 μsec delay drives the data record trigger. The delay allows the output at V(t) to rise to its peak amplitude before informing associated equipment that the output data is ready for use.

x. The data record trigger output signals associated equipment that the output from the Model 153 is present at the output jack, V(t), and ready to be used. The data record trigger is a 0.5 μsec wide pulse that starts 4 μsec after strobe time.

3-3 CIRCUIT DESCRIPTION

a. Measurement Interval. The measurement interval is initiated by a trigger applied to the 50Ω panel-mounted TRIGGER IN jack. The trigger signal may be of either polarity as selected by the panel-mounted TRIGGER POLARITY switch. The trigger sensitivity adjustment permits triggering from signals of 100 mv to 20v in amplitude. The triggering signal is applied to the discriminator through the balun transformer, T201. T201 is made up of two turns of the input coax looped through a ferrite core. The purpose of T201 is to provide push-pull drive from the single-ended input. Triggering is accomplished by a positive-going waveform at pin 1 of the printed circuit board.

b. Trigger Discriminator. The trigger discriminator is a push-pull amplifier pair made up of Q1 and Q2. R23 and R65 from the -15v supply provides a

constant 10 ma of emitter current to be shared by Q1 and Q2. In the quiescent condition with no trigger signal applied, Q1 conducts a little more than 5 ma, and Q2 conducts a little less than 5 ma, determined by the difference in their individual emitter resistor, R22 and R24. Q1 and Q2 each have a tunnel diode in their collector circuit which will snap to its high voltage state when driven with 10 ma or more. When a trigger signal is applied which agrees with the trigger polarity selector switch and sensitivity setting, Q2 increases conduction beyond 5 ma, and Q1 reduces conduction below 5 ma.

c. Trigger Shaper. The trigger shaper is made up of the tunnel diode, CR4, and the voltage-amplitude discriminator pair, Q4 and Q5. In the quiescent condition, with no trigger applied, the tunnel diode CR4 is in its low voltage state (100 mv), Q4 is not conducting and Q5 conducts all of the common emitter current through R5 from the +15v supply. The divider made up of R7 and R8 establishes the base voltage of Q5 at 250 mv below the +5v supply. The two voltage states of CR4 are 100 mv and 500 mv. Q4 does not conduct when CR4 is in its low voltage state. Q4 conducts all of the common emitter current through R5 when CR4 is in its high voltage state.

Triggering is accomplished when CR4 snaps from its low voltage state to its high voltage state. The current threshold for CR4 is 10 ma. A constant 5 ma is furnished to CR4 through R26 from ground. The remainder of the current for CR4 is collector current from Q2 which is normally less than 5 ma. When a positive-going trigger signal is applied to the base of Q2, the increase in collector current pushes CR4 over its current threshold into its high voltage state and causes current to switch from Q5 to Q4.

During the 1 ms hold-off interval following trigger, Q3 conducts at saturation and effectively bypasses CR4. During this hold-off interval, even if trigger signals are applied to the trigger discriminator pair, collector current for Q2 is conducted through Q3 and the tunnel diode CR4 remains in its low voltage state. Triggering cannot occur again until the hold-off clamp, Q3, is turned off making current available to CR4.

d. Bistable Multi. The bistable multi, made up of Q6 and Q7, is switched by collector current from Q4. The bistable multi remains switched for the first half of the hold-off interval. The quiescent condition before triggering is with Q6 conducting and Q7 not conducting. Collector current from the trigger shaper, Q4, pulls the base of Q6 in a positive direction turning off Q6 and turning on Q7.

e. Ramp Gate. The ramp gate is a current switching output stage for the bistable multi. When the bistable multi is in its quiescent condition, prior to trigger, Q9 conducts all of the common emitter current through R32 from the -15v supply. Q10 does not conduct in the quiescent condition. When the bistable multi switches as a result of triggering, Q9 turns off and Q10 conducts all of the common emitter current. There are two outputs from the ramp gate. Prior to triggering, Q9 provides current to the hold-off switch. During the first 500 μs of the hold-off interval when the bistable multi is switched, Q9 turns off the current to the hold-off switch. Prior to triggering, when Q10 is not conducting, R35 provides base current for the ramp generator. When triggering occurs and Q10 conducts, the collector of Q10 is pulled down to one junction drop below ground, defined by the clamp diode CR10. During the first 500 μs of the hold-off interval, R35 does not provide base current to the ramp generator.

f. Hold-off Switch. The hold-off switch is made up of Q11, Q12, and Q13. The timing capacitors, C3 and C18, define the hold-off interval. Q12 and Q13 are a current switching pair. They share a common emitter current through R10 from the +25v supply. The base voltage of Q13 is defined by the +15v supply. The base voltage for Q12 is above or below the 15v supply, depending on whether or not Q11 conducts. In the quiescent condition before triggering, Q11 conducts the current supplied from the ramp gate, Q9. The base of Q11 is referenced to the +5v supply through R9, and Q11 acts as an emitter follower to hold the voltage on C3 and C18 to 1 junction drop below the +5v supply. Collector current from Q11 holds the base of Q12 below the +15v supply and Q12 conducts all of the current supplied through R10 from the +25v supply. In the quiescent condition Q13 does not conduct.

When triggering occurs; the current supplied by Q9 is turned off, Q11 stops conducting, the base of Q12 goes more positive than the +15v supply, and Q13 conducts all of the current through R10 from the +25v supply. C3 and C18 charge toward the +25v supply through R14 and R13.

The time constant defined by C3, C18, R14 and R13 determines the first half of the hold-off interval. When C3 and C18 charge to a voltage positive enough to cause Q8 to conduct, the bistable multi is switched back to its quiescent condition and Q9 again supplies current. The time constant defined by C3, C18 and collector current from Q9 determines the second half of the hold-off interval. Collector current from Q9 discharges C3 and C18 back down to their quiescent voltage of less than 5v. The discharge current provided to C3 and C18 is approximately equal to the charge current provided through R13. The charging time of C3 and C18 defines the first half of the hold-off interval, and the discharge time defines the second half. When C3 and C18 have discharged below +5v, Q11 goes back into conduction providing base current to Q12. Q12 conducts the common emitter current from R10, and Q13 is turned off. The hold-off interval is made up of two 500 μs intervals. The first interval is with the bistable multi switched, Q9 turned off, C3 and C18 charging in a positive direction. The second 500 μs interval is with the bistable multi switched back to its quiescent condition and Q9 discharging C3 and C18. The hold-off interval is not terminated until C4 and C18 are discharged below 5v and Q11 goes back into conduction.

g. Hold-off Clamp. The hold-off clamp, made up

of CR1 and Q3, effectively bypasses the tunnel diode CR4 during the hold-off interval. The quiescent condition of the hold-off clamp before triggering is with CR1 in its high voltage state and Q3 not conducting. In this condition, collector current from Q2 in the trigger discriminator circuit plus the current from R26 is available to drive CR4. During the hold-off interval when Q13 is conducting, collector current from Q13 holds CR1 in its low voltage state and causes Q3 to conduct at saturation. When the hold-off interval is over and Q13 is turned off, CR1 will snap back to its high voltage state, providing Q1 in the trigger discriminator circuit is conducting its quiescent collector current. If the initial trigger signal is still present on the trigger discriminator when hold-off is terminated, Q2 is still conducting more than its quiescent 5 ma, Q1 is conducting less than its quiescent 5 ma, and CR1 will not snap back to its high voltage state. The trigger signal on the trigger discriminator must revert to near zero after the hold-off interval for Q1 to conduct its quiescent current before CR1 will snap back to its high voltage state and turn off Q3. This provision is incorporated to prevent a wide trigger signal from initiating more than one measurement cycle. If the trigger discriminator is in its quiescent condition when the hold-off interval is over, collector current from Q1 plus the current from R3 is sufficient to snap CR1 back to its high voltage state and turn off Q3. Current from Q2 is then available to CR4 to initiate a new trigger.

h. Ramp Generator. The ramp generator includes Q14, Q15 and the charging capacitors, C6, C10, C11 and C12. Q15 is a constant current source of about 20 ma from the +15v supply. Before triggering, Q14 conducts at saturation holding its collector near ground because of the base current supplied to it by R35 in the ramp gate circuit. When triggering occurs, Q10, in the ramp gate circuit, conducts pulling the base of Q14 one junction drop below ground. Q14 is turned off for the first half of the hold-off interval (500 μs following trigger) and the constant current provided by Q15 charges C6. The waveform provided to the ramp comparitor by C6 is a linear positive-going ramp. The ramp starts near ground and runs up to +5v in the time determined by the ramp range selector. The ramp continues to charge past the end of the range to about +6v where it is clamped by the counter driver. The ramp stays at the +6v level for 500 μs following trigger. At the end of the 500 μs when the ramp gate switches back to its quiescent condition, Q14 again conducts at saturation and discharges the ramp range capacitors back to near ground.

i. Ramp Range Selector. The ramp range selector is made up of Q16, Q17, Q18 and the charging capacitors C6, C10, C11, and C12. The inputs to the ramp range selector are from the front panel range selector switch or from external programming logic through the buffer amplifiers on the buffer board. When base current is provided to Q16, Q17, or Q18, the respective charging capacitor, C10, C11, or C12, in their collector circuit, is in parallel with the charging capacitor, C6, modifying the time interval required for the ramp to reach its full scale voltage level of +5v. The ramp ranges are not mutually exclusive and care must be taken in programming to avoid two simultaneous ranges. The clamp diodes CR20, CR21, and CR22 provide a discharge path for their respective charging capacitors.

j. Delay Analog Buffer. The delay analog buffer is a voltage-feedback stabilized amplifier with a voltage gain of 2. The input of the delay analog buffer is a voltage between 0 and +5v which determines the portion of the selected delay range to be used. Zero voltage input provides no delay and +5v provides full scale delay on the selected delay range. The output of the delay analog buffer makes the delay analog voltage available at the DELAY ANALOG OUT jack from a 1 kΩ source impedance. The output of the delay analog buffer also provides the dc reference voltage to the ramp comparitor.

The input to the delay analog buffer is selected by the panel-mounted DELAY MULT. SOURCE switch. The delay analog voltage source can be: (1) a panel-mounted 10 turn dial, (2) the DELAY ANALOG IN jack or, (3) the output of the D/A converter. A dc offset adjustment is provided in the output of the delay analog buffer so the dc level to the ramp comparitor will agree with the ramp voltage.

The delay analog buffer is made up of Q1, Q2, Q3, and Q4. Q1 and Q2 are connected as a voltage-amplitude discriminator pair which share a common source of emitter current through R8 from the -25v supply. Q1 and Q2 each conduct about 1 ma. When a + voltage is applied to the base of Q1, the increase in collector current in Q1 provides base current to Q3. The collector current of Q3 pulls the base voltage of Q2 up to equal the base voltage of Q1. The current flow through R11, required to hold the base voltage of Q2 equal to the base of Q1, must also flow through R10. Since R10 and R11 are the same value, the voltage at the collector of Q3 is twice the voltage at the base of Q2. The network R12 and R13 provides for forcing additional current, either + or -, through R10. This permits a small adjustment in output dc level to compensate for the difference in the base-emitter junction drops of Q1 and Q2.

When the delay analog output is used to drive the delay analog input of another Model 153, the 1 kΩ input impedance of the second Model 153, together with R15, make up a 2:1 divider. This divider and the 2X voltage gain provided by the delay analog buffer makes the input voltage to the second Model 153 the same as the delay analog input voltage to the first Model 153.

When the delay analog input has selected the full delay range, +5v is present at the input of the delay analog buffer. Since the delay analog buffer has a voltage gain of 2, the voltage at the collector of Q3 will be +10v. The reference voltage provided to the ramp comparitor will be +5v (about 0.5v of fixed dc offset and 4.5v of dynamic control voltage). The voltage divider made up of R16 and R17 on the buffer board and R43, R42, and R44 on the trigger board divides the dynamic control voltage output of the delay analog buffer down to 4.5v as a reference for the ramp comparitor. Q4 and its associated components make up a constant current

source of about 3 ma. Since the delay ramp starts at +0.5v, it is necessary to offset the delay analog reference voltage by an equal amount.

k. Range Ramp Comparitor. The range ramp comparitor is a voltage-amplitude discriminator made up of Q19, Q20, Q21, and Q22. The inputs to the ramp comparitor are the delay ramp at the base of Q19 and the delay analog reference voltage at the base of Q20. The voltage amplitude discriminator pair, Q19 and Q20, share a common source of emitter current through R38 from the +25v supply. Before trigger occurs, the base of Q19 is held clamped at +0.5v by Q14 in the ramp generator. The base of Q20 is some voltage between +0.5v and +5v determined by the delay analog input through the delay analog buffer. Q19 conducts all the emitter current avialable and Q20 is turned off. Q22 and Q21 are output amplifiers for Q19 and Q20. Q22 and Q21 share a common source of emitter current through R45 from the -15v supply. When Q19 is conducting, before triggering, Q22 conducts all the current available through R45, and Q21 is turned off.

When triggering occurs, the voltage at the base of Q19 runs up in a positive direction with a slope determined by the ramp range selector. When the voltage at the base of Q19 is equal to the voltage at the base of Q20, Q20 starts to conduct providing base current to Q21. Collector current from Q21 pulls the base of Q20 sharply negative to speed up the current switching from Q19 to Q20. Current switching from Q19 to Q20 occurs at a time interval after trigger determined by the ramp range selected and the dc delay analog programmed. When conduction is transferred from Q19 to Q20, conduction is also transferred from Q22 to Q21. The interruption of current flow through L1 in the collector circuit of Q22 produces a sharp positive spike which triggers the delayed pulse generator.

l. Delayed Pulse Generator. The delay pulse generator is a one-shot multivibrator which produces a 200 ns delayed pulse starting at the end of the programmed delay interval. The leading edge of the delayed pulse triggers the strobe generator and the trailing edge triggers the memory gate generator.

The delayed pulse generator is made up of the one-shot multivibrator, Q23 and Q24, and the output amplifier pair, Q25 and Q26. The quiescent condition for the delayed pulse generator is with Q23 and Q26 conducting, and with Q24 and Q25 turned off.

The quiescent base voltage for Q23 is established by the voltage divider, R47, CR15A, R18A and the clamp diode CR17. The clamp diode CR17 holds the anode of CR15A at one junction drop below ground. This sets the quiescent base voltage for Q23 at 5.7v. Collector current from Q23 forward biases the clamp diode CR16 holding the anode of the zener diode CR15B at one junction drop above ground. This sets the quiescent base voltage of Q24 and Q25 at +6.9v. Q23 conducts all of the current supplied through R49 and R50 from the +15v supply. Q23 also conducts the current supplied through R51 and CR18 from the +15v supply.

When the one-shot multivibrator is triggered by a positive pulse from the ramp comparitor, Q23 turns off. The collector voltage of Q23 drops below ground, providing drive to the base of Q24. Q24 conducts the current through R51 from the +15v supply and also the current through R50 and R49 through C9. C9 can support the current through R49 and R50 for 200 ns after which time the emitter of Q23 has gone far enough positive for Q23 to go back into conduction, turning off Q24 and reverting the one-shot multivibrator back to its quiescent condition.

In the quiescent condition, Q26 conducts the current supplied through R53 from the +15v supply and Q25 is turned off. During the 200 ns delayed pulse, Q25 conducts the current supplied through R53 and Q26 is turned off. This produces a positive-going delayed pulse at the collector of Q25 and a negative-going delayed pulse at the collector of Q26. The leading edge of the output from Q25 triggers the strobe generator. The trailing edge of the output from Q26 triggers the memory gate generator.

m. Counter Driver. The purpose of the counter driver is to clamp the delayed ramp when it has reached +6v and to produce an output to increase the digital counter by 1 bit. The counter driver is made up of Q27 and Q28.

The quiescent condition of the counter driver is with both Q27 and Q28 turned off. The base of Q27 is held at +5v by the divider made up of CR6 and R19. The range ramp drives the emitter of Q27. With Q27 not conducting, the base of Q28 is held at one junction drop below ground by the divider R18 and CR7. The collector of Q28 is at a + voltage set by the divider R2 and R21. When the range ramp runs up to one junction drop more positive than the zener diode CR6, Q27 conducts as a grounded base amplifier and the delay ramp is clamped at this voltage for the remainder of the first half of the 1 ms hold-off interval. Collector current from Q27 provides enough base current to saturate Q28. The resulting negative-going collector waveform of Q28 provides the drive to increase the digital counter by 1 bit.

n. BCD Counter. The BCD (binary coded decimal) counter is a synchronous counter made up of integrated-circuit JK flip-flops and logic gates. The input to the counter is the waveform from the counter driver which increases the counter by one bit at the end of each range ramp. The output of the counter is 12 diode-isolated logic lines with conventional 1-2-4-8 BCD logic. That is, when the counter is in the "0" state, all logic lines are 0v. Logic "1" is +3v.

Twelve J K flip-flops are used, 2 contained in each of 6 IC packages (IC 10 through IC 15). The remaining packages on the board, IC 1 through IC 9, are logic gates.

The operational characteristics of the J K flip-flops are: (1) if the S/C inputs are at 0v when a bit is applied to the T input, the flip-flop will change states; and (2)

if the S/C inputs are + when the bit is applied to the T input, the flip-flop will not change states.

The operational characteristics of the logic gates are: (1) if any input to a single gate is +, the output will be 0, and (2) if all inputs to a single gate are 0, the output will be +.

The input bit from the counter driver is applied to the T input of all 12 flip-flops in parallel. The logic gates controlling the S/C inputs determine whether or not a particular flip-flop will accept the trigger and change states.

Two fundamental requirements of a binary counter are: (1) the low order stage must change states with each input bit, and (2) each of the remaining stages must change states when all lower order states are changing from "1" to "0". In addition to these fundamental binary requirements, if the output is to be BCD, all stages within a single decade must be in the "0" state as a result of the 10th input bit.

The first binary requirement is met by simply grounding the S/C inputs on the first stage. The S/C inputs of the first stage are always 0v, and the first stage will change states with each input bit.

The second binary requirements (all remaining stages change states when all lower order stages switch from "1" to "0") is met by making the S/C inputs of each stage an AND term of the $\overline{Q}$ output of all lower order stages. Therefore, an input bit can switch the state of a stage only if all lower order stages are "1" when the input bit is applied.

The third requirement (to make the full decade "0" as a result of the 10th bit) is accomplished by inhibiting the "2" stage and forcing the "8" stage on the 10th input. The "1" stage normally goes to "0" on the 10th input bit, so no extra influence is needed. The "2" stage is at "0" after the 9th input bit, but it will normally switch on the 10th bit if not prevented. The "4" stage is at "0" after the 9th bit and will normally stay at "0" after the 10th bit, so no additional influence is needed. The "8" stage is at a logic "1" after the 9th bit, and will not normally revert to "0" until the 16th bit. The "8" stage must be switched to "0" by the 10th input bit.

The logic levels in Fig. 3-1 show the output voltage levels from each stage in the first decade of count.

The S/C inputs to the low order stage, pins 7 and 5 of IC 10A, are permanently grounded. Therefore the low order stage switches states on each input bit.

The logic at the S/C input to the remainder of the stages is an AND term of the $\overline{Q}$ output of all lower order stages. Any stage can switch states on an input bit if all lower order stages are a logic "1" when the input bit is applied.

The output of the logic gate 1C is up if the first decade is "9" (simultaneously "1" and "8"). This output inhibits the 2 stage from switching and permits the 8 stage to switch on the 10th input bit, thus causing the first

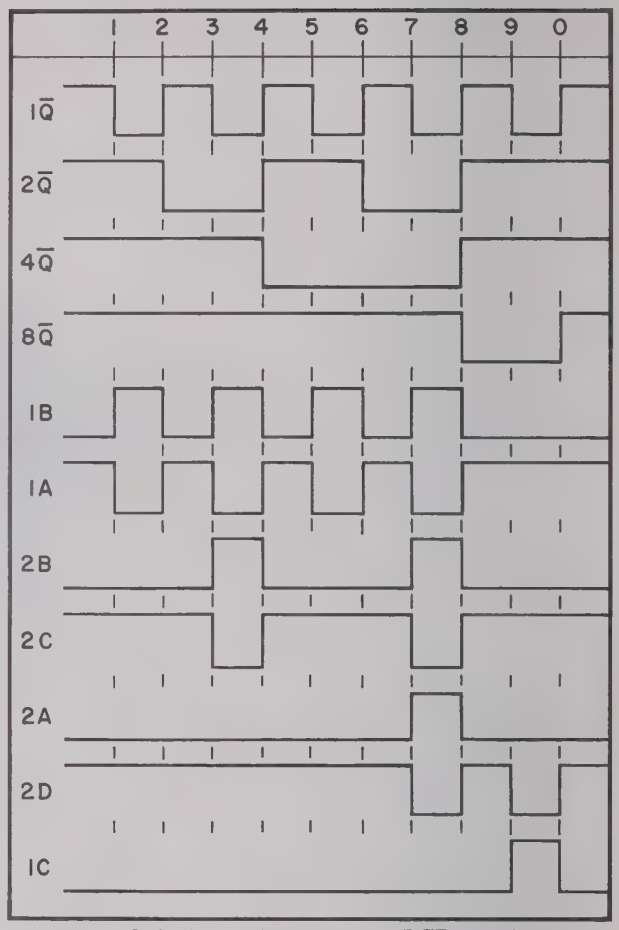


Fig. 3-1 Logic levels in the BCD counter

decade to assume the "0" state after the 10th input bit.

The second decade functions the same as the first decade except the logic gate 1D inhibits the entire second decade on all input bits except the first decade overflow bits.

Similarly the third decade functions the same as the first two except that the logic gates 3A and 3B inhibit the third decade on all bits except the second decade overflow bits.

There are 12 output transistors, Q1 through Q12. Each of the output transistors drives one of the logic lines. The $\overline{Q}$ output of each counting stage provides base current for its respective output transistor when that stage is in the "0" state. When an output transistor is conducting, its collector is clamped near ground. When the counting stage is in the "1" state, no base current is supplied by the $\overline{Q}$ output, and the output collector goes positive to the power supply voltage. Therefore the 12 logic lines carry true BCD logic. That is, logic "1" is +3v, and logic "0" is 0v.

o. D/A Converter. The D/A converter is a 3-decade digital-to-analog converter. The inputs to the D/A

converter are the 12 BCD logic lines from the digital counter or from the external programming connector, J302. The output of the D/A converter is a voltage between 0 and +5v proportional to the value of the number represented by the BCD code.

The D/A converter is made up of 12 saturating switches, each with a current weighting resistor proportional to the numerical value of its logic line, and a common current-summing output stage.

Since the 12 saturating switches are identical, except for the value of the current weighting resistor, only the "1" switch will be discussed. The "1" saturating switch consists of Q39, Q38, and their associated components. If the "1" logic line is down (0v) neither Q39 nor Q38 have base current, and neither conducts. If the "1" logic line is up (+3v), Q39 conducts supplying base current to Q38. Q38 saturates, and collector current is determined by the value of R37, the current weighting resistor. Each of the 12 saturating switches provides current to the output stage proportional to the numeric value of its logic line.

The output stage, Q4, is a grounded base amplifier. Emitter current for Q4 is the sum of the 12 weighted currents plus a constant idling current supplied through R12 and R13 from the +15v supply. The collector load for Q4 is R6 and R7 on the buffer board. The collector is returned to a Thevenin-equivalent of -0.25v to compensate for the effect of the idling current.

The D/A converter board may be rewired to latch and hold, or to accommodate other than 1-2-4-8 BCD logic. Contact your E-H Representative or the factory for exact details.

p. Strobe Generator. The strobe generator gates the sampling bridge on during the first 4 ns of the delayed pulse. The strobe generator consists of Q6, Q7, Q8, Q9, Q10, Q11, and the pulse transformer T1. In the quiescent condition, each of the three pairs have one transistor conducting and the other turned off. Q7 is conducting because of the dc level provided to its base by the delayed pulse generator. Q6 is turned off. The clip line is a dc short-circuit between the collectors of Q6 and Q7. The junction drop across CR5 holds the base of Q8 one junction drop more negative than the base of Q9, therefore Q9 conducts and Q8 is turned off. Q9 provides base current to Q11, so Q11 conducts and Q10 is turned off.

The timing element in the strobe generator is the clip line connected between the collectors of Q6 and Q7. In the quiescent condition, R48 and R50 are parallel collector loads to Q7 with the current through R50 flowing through the clip line. When the delayed pulse switches current from Q7 to Q6, R48 and R50 are parallel collector loads to Q6 with current from R48 flowing through the clip line. When Q6 is conducting, current flow through the clip line is in the opposite direction from the quiescent condition. During the 4 ns required to discharge the clip line and charge it back in the opposite direction, the surge impedance of the clip line can be considered as two 50Ω resistors; one from the collector of Q6 to ground, the other from the collector of Q7, to ground. After the 4 ns transistion time, the clip line is again a dc short-circuit between the collector of Q6 and Q7.

The leading edge of the positive-going delayed pulse turns off Q7 and turns on Q6. For 4 ns following current-switching, Q6 and Q7 each have an effective collector impedance of 25Ω. When the 30 ma through R51 is switched from Q7 to Q6, the collector of Q7 goes negative 0.75v and the collector of Q6 goes positive 0.75v. These voltages cause Q8 to conduct and Q9 to turn off. Current is switched from Q11 to Q10 and the current flow through the primary of T1 is reversed for 4 ns. The output pulse from T1 gates on the sampling bridge.

The voltage divider made up of R23, R22, R21, R20, and R19 provides back bias for the sampling bridge diodes. For proper adjustment of R23, refer to the calibration procedure in Section 4.

q. DC Offset Amplifier. The dc offset amplifier provides the reference level for the sampling bridge and the first memory amplifier. The measurement made by the Model 153, is the voltage difference between the input signal at strobe time and the dc offset voltage. The output of the dc offset amplifier is equal to the externally applied dc offset input between the limits of -1v and +1v.

The dc offset amplifier is a voltage-feedback stabilized amplifier made up of Q15A, Q15B, Q12, Q13, and Q14. The dc offset input is applied to the base of Q15A. Q15A and Q15B are connected as a voltage-amplitude discriminator pair. They share a common source of emitter current through R25 from the -15v supply. Q15A provides base current to Q14, Q15B provides base current to Q12, and Q12 in turn drives Q13. The phase relationship through the amplifier is such that the collector current of Q13 pulls the base voltage of Q15B up to equal the voltage at the base of Q15A. The current flow through R36 and R35 necessary to hold the base of Q15B equal to the base of Q15A must also flow through R34. The dc voltage at the collector of Q13 is 1.3 times the dc voltage at the base of Q15B. The voltage at the collector of Q13 provides the reference level for the feedback resistors in the first memory amplifier. The voltage at the base of Q15B provides the reference voltage for the sampling bridge through R2.

r. First Memory Amplifier. The first memory amplifier is a high-input-impedance operational amplifier with a voltage gain of 4X. At the end of the programmed delay interval, the sampling bridge is turned on for 4 ns, connecting the applied signal to the input of the first memory amplifier. The input time-constant, while the sampling bridge is turned on, is approximately 0.35 ns. This time-constant, together with the 4 ns strobe width, permits C1 to charge to the full signal voltage present on the bridge at the end of strobe time. After strobe time, when the input to the first memory amplifier is isolated from the signal source, the input time-constant is about 50 μs.

The first memory amplifier is made up of Q1A, Q1B, Q2, Q3A, Q3B, Q4, and Q5. The signal input is at the gate of Q1A. The feedback voltage is applied from the output through the voltage divider, R16-R32, to the gate of Q1B. Within the voltage-gain limitations of the amplifier, the voltage at the gate of Q1B is held equal to the voltage at the gate of Q1A. The amplifier has a voltage gain of 4X set by the ratio of R32 to R16 + R32.

When a dc offset voltage is applied to the input of the first memory amplifier at the gate of Q1A, an equal dc offset must be applied to the gate of Q1B so the output of the first memory amplifier will be 0v with no input signal applied. The ratio of R16 to R32 dictates that the voltage applied to the bottom of R32 must be 1.3 times the voltage applied to the gate of Q1B. Since it is desirable for the voltage at the gate of Q1B to equal the voltage at the gate of Q1A, the voltage gain of the dc offset amplifier must be 1.3. The feedback divider, R16 and R32, are referenced to a point in the dc offset amplifier which is 1.3 times the dc offset voltage.

s. Memory Gate Generator. The memory gate generator is a one-shot multivibrator which is triggered by the trailing edge of the delayed pulse. It generates a 1.2 μs gate which turns on the memory gate bridge. By starting the memory gate from the trailing edge rather than the leading edge of the delayed pulse, the first memory amplifier is allowed 200 ns to reach its peak amplitude before the second memory amplifier samples its output.

The one-shot multivibrator is Q12 and Q13. Q10 and Q11 make up a current-switching output stage. In the quiescent condition, Q13 is conducting and Q12 does not conduct. The reference voltage for the zener diode, CR9B, is one junction drop below ground set by the clamp diode, CR13. The reference voltage for the zener diode, CR9A, is one junction drop above ground set by the clamp diode, CR11. In the stable state, the base of Q13 is two junction drops more negative than the base of Q12. Q13 conducts the current through R55 and R56 from the +15v supply, and also the current through R53 and CR10 from the +15v supply.

The trailing edge of the delayed pulse produces a positive voltage spike across L2, which is coupled through CR12 and CR9B turning off Q13. The resulting negative waveform at the collector of Q13 turns on Q12. Q12 conducts the current through R53 and the current through C11, R55, and R56. As C11 charges, the emitter of Q13 goes in a positive direction until the base-emitter junction of Q13 is forward biased. When Q13 goes back into conduction, the positive going waveform at the collector of Q13 turns off Q12, and the multivibrator reverts to its stable state. The period of the multivibrator is determined by the time-constant of C11, R55, and R56.

The output stage, Q10 and Q11, is a current commutating pair. In the quiescent condition, Q11 conducts the current through R39 from the +15v supply, and Q10 does not conduct. During the 1.2 μs that the one-shot multivibrator is switched, Q10 conducts and Q11 is turned off. Collector current from Q10 through the pulse transformer, T1, turns on the memory gate bridge for 1.2 μs.

t. Memory Gate Bridge. The memory gate bridge (CR1A, CR1B, CR1C, and CR1D) connects the output of the first memory amplifier to the input of the second memory amplifier for 1.2 μs starting 200 ns after strobe time.

u. Second Memory Amplifier. The second memory amplifier is a high-input-impedance operational amplifier with a voltage gain of 2.5X. The input to the second memory amplifier is connected to the output of the first memory amplifier by the memory gate bridge for 1.2 μs starting 200 ns after strobe time.

The second memory amplifier is made up of Q1A, Q1B, Q2, Q3A, Q3B, Q4, and Q5. The signal input is at the gate of Q1A. The feedback voltage is applied from the output through the divider (R18-R19-R20) to the gate of Q1B. Within the open-loop voltage gain limitations of the amplifier, the voltage at the gate of Q1B is held equal to the voltage at the gate of Q1A. The voltage gain of the amplifier is set by the ratio of R19 + R20 to R19 + R20 + R18. The holding time-constant of 250 ms is set by the input capacitor, C2, and the input resistor, R3 through R7.

v. Output Amplifier. The output amplifier includes the OUTPUT GAIN selector switch, S202, and an operational amplifier with a voltage gain of 10X. The operational amplifier is made up of Q6, Q7, Q8, and Q9.

When the OUTPUT GAIN selector switch is in the X1 position, the output of the second memory amplifier is attenuated by a factor of ten by the voltage divider, R23-R201-R202. The 10X voltage gain of the memory amplifiers together with the 10X attenuation at the output makes the voltage available at the output connector, V(t), equal to the applied signal voltage at strobe time.

When the OUTPUT GAIN selector switch is in the X10 position, the output of the second memory amplifier is connected directly to the output connector, V(t). The voltage gain of the memory amplifiers provides the overall voltage gain of 10X.

When the OUTPUT GAIN selector switch is in the X100 position, the output of the second memory amplifier drives the input of the output amplifier, and the output amplifier drives the V(t) output connector.

The input to the operational amplifier is the base of Q6. The feedback voltage is applied from the output through the divider, R33-R34, to the base of Q7. The voltage gain of the operational amplifier is set by the ratio R34 to R33 + R34.

w. 3 μs Delay Circuit. The 3 μs delay circuit is a one-shot multivibrator made up of Q14 and Q15. It is triggered by the trailing edge of the memory gate waveform, and drives the date record trigger output stage. The purpose of the 3 μsec delay is to permit risetimes through the memory amplifiers before signaling

auxiliary equipment that the output voltage is ready for use.

In the quiescent condition, Q14 conducts at saturation, holding its collector near ground. Q15 does not conduct since it has no source of base current. The negative-going 1.2 μs gate at the collector of Q11 is differentiated by C7 and R64. The positive-going spike at the end of the 1.2 μs gate is coupled through CR6 and turns off Q14. The negative-going waveform at the collector of Q14 provides base current to Q15 through R47. Q15 saturates and pulls its collector voltage up to ground. The positive-going waveform at the collector of Q15 is coupled to the base of Q14 through C8. Q14 remains turned off for 3 μs determined by the time-constant of C8 and R42. When C8 has discharged far enough for the base of Q14 to go one junction drop below ground, Q14 goes back into conduction and pulls its collector back up to ground. When the collector of Q14 returns to ground, Q15 turns off and the one-shot multivibrator returns to its quiescent condition.

x. Data Record Trigger. The data record trigger output stage is Q16. It provides a 0.5 μs pulse at the end of the 3 μs delay (approximately 4 μs after strobe time). In the quiescent condition, Q16 does not conduct. The collector is at some positive voltage determined by R51 and the load connected to the DATA RECORD TRIGGER output connector J302.

The negative-going waveform at the collector of Q15 is differentiated by R49 and C10. The positive-going spike at the trailing edge of the 3 μs delay waveform turns on Q16 and its collector is pulled to ground for about 0.5 μsec.

y. Regulated Power Supplies. Five regulated power supplies provide operating voltages to the circuitry in the Model 153.

The +25v regulated power supply is made up of Q1, Q2, Q3, Q101, and the zener reference CR5. Q1 and Q2 are a voltage-amplitude comparitor pair, Q3 provides open-loop voltage gain, and Q101 is the series regulating element. The voltage at the base of Q1 is held to +9.0v by the zener reference, CR5. A proportional sample of the +25v supply is applied to the base of Q2 through the divider, R5-R6-R7. The phase relation through the amplifier is such that the output at the emitter of Q101 is out of phase with the error voltage at the base of Q2. The open-loop gain of the amplifier holds the output voltage at the +25v buss to whatever voltage is necessary to minimize the error voltage at the base of Q2.

The +15v regulated supply is made up of Q7, Q8, Q9, Q103, and the zener reference CR5. With the exception of the component values, the +15v supply functions in the same manner as the +25v supply described above.

The -15v supply is made up of Q10, Q11, Q12, and Q104. Q10 and Q11 are the voltage-amplitude discriminator pair, Q12 provides open-loop gain, and Q104 is the series regulating element. The base of Q10 is referenced to ground. Since R27 and R28 are equal values, the -15v supply must be as much negative as the +15v supply is positive to provide the base of Q11 with a voltage equal to the base of Q10. The open-loop gain of the amplifier pulls the voltage at the emitter of Q104 in the direction that will minimize the error voltage between the base of Q11 and the base of Q10. The exact voltage output of the -15v supply is dependent on the output of the +15v supply.

The -25v supply is made up of Q4, Q5, Q6, and Q102. Q4 and Q5 are the voltage-amplitude discriminator pair, Q6 provides open-loop gain, and Q102 is the series regulating element. The base of Q4 is referenced to ground. The voltage at the base of Q5 is established by the divider, R12-R13 between the +25v supply and the output of the -25v supply). As with the -15v supply discussed above, regulation of the -25v supply depends on regulation of the +25v supply.

The +3.6v supply is made up of Q13, Q105, and the zener reference CR6. CR6 provides the reference voltage, Q13 is the voltage comparitor and provides the open-loop gain, and Q105 is the series regulating element. The base of Q14 is held at +4.3v by the zener reference CR6. Collector current from Q13 provides base current for Q105. As the collector of Q105 pulls positive, it robs current from the emitter of Q13. A point of equilibrium is reached with the emitter of Q13, one junction drop below the zener reference voltage.

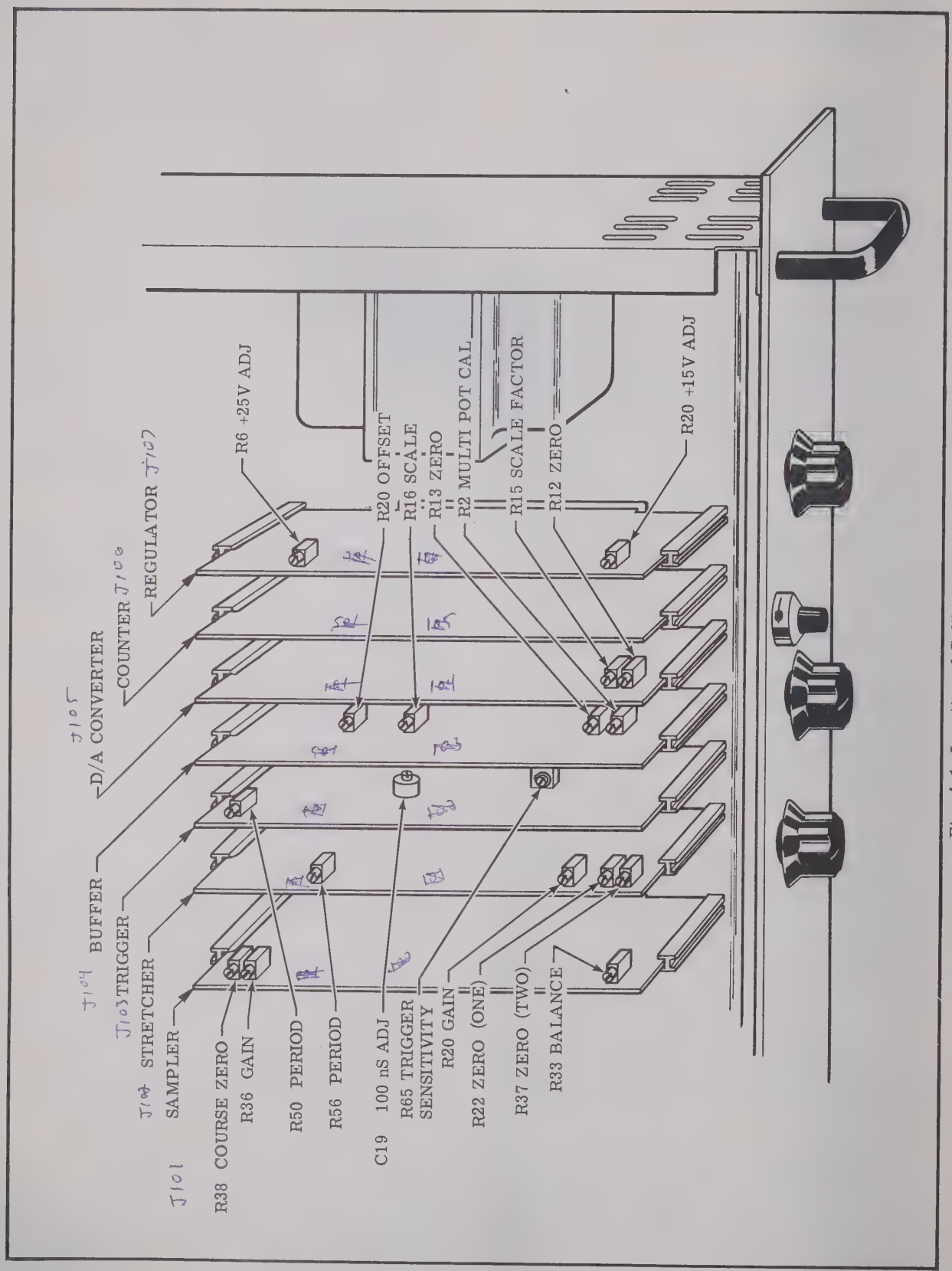


Fig. 4-1 Location of Calibration Adjustments

SECTION 4
MAINTENANCE

4-1 GENERAL

The E-H Model 153 Strobing Voltmeter requires a minimum amount of maintenance; however, normal aging of electronic components may eventually cause abnormal operation. Therefore, general maintenance and trouble shooting information is included in this section as a guide to restoring the instrument to normal operation.

4-2 ROUTINE MAINTENANCE

A regular program for maintenance and inspection every four to six months is recommended to effectively minimize equipment down time. As part of the regular maintenance and inspection procedure, the instrument should be carefully checked in the following manner:

a. Remove the Model 153 cover panels.

b. Make a thorough inspection of all wiring and cables. Check for frayed, loose, or burned wires.

c. Check the physical integrity of all components. Look for evidence of burning or cracking, loose solder connections, leakage of insulation compounds, and general physical damage.

d. Check all switches and controls for loose or broken terminals, tight or sticking shafts, etc.

e. If the internal panel surfaces and components have an excessive amount of dust or lint deposited on them, use a low pressure stream of air to remove the foreign material.

CAUTION

Do not clean the circuit boards or small internal components with a wiping cloth or solvents, since damage to the circuits may result.

f. Wipe the external surfaces of the instrument with a soft, damp cloth to remove dirt, fingerprints, and other foreign materials.

g. Remove and clean the metal air filter. The filter may be washed in soapy water. Rinse in clear water, dry and replace the filter on the instrument. The filter must be kept clean and unrestricted.

h. If repairs are made to the instrument, or if a performance verification indicates that it is not operating within the tolerances stated in Section 1, a complete calibration procedure as outlined in this section should be performed. Before attempting the calibration procedure, read Section 3 of this instruction manual. A working knowledge of the circuitry is necessary to insure optimum performance of the instrument.

4-3 CALIBRATION PROCEDURE

a. Equipment required.

(1) Time mark generator - Tektronix Type 184 or equal.

(2) Real time oscilloscope - Tektronix Type 541 or equal.

(3) Voltmeter 1% accuracy - Simpson 262 or equal.

(4) Resistors 1/2 watt, 5%; 30 k, 3 k, 270Ω.

(5) Pulse Generator, E-H Model 139B or equal.

b. Precautions. Component density on the etched circuit boards is high. Leads are close together and one side of the circuit board is a ground plane. Take care, when attaching voltmeter leads, oscilloscope probes, etc. that the probe touches only the point to be tested. Solid state junctions can easily be destroyed by allowing the test lead to touch two points or one point and ground.

For best results, it is recommended that the entire calibration procedure be performed in the sequence stated.

c. Adjust and Check regulated supplies.

(1) Measure the +15v supply at pin 6 of the printed circuit board sockets, and adjust R20, "+15v adj", for +15v ±1%. ±.015

(2) Measure the +25v supply at pin 15 of the printed circuit board sockets, and adjust R6, "+25v adj", for +25v ±1%. ±.025

(3) Check the -15v supply at pin 7 for -15v ±3%. ±.045

(4) Check the -25v supply at pin 14 for -25v ±3%. ±.045

(5) Check the +3.6v supply at pin 1 of the regulator board socket for +3.6v ±10%. ± .36 J107

d. Adjust delay analog buffer.

(1) With the DELAY MULT. SOURCE switch on INT, and the DELAY MULTIPLIER set to 10.00 (not full clock-wise), measure the voltage at pin 9 of the

buffer board socket, J104. Adjust R2, "Multi pot cal", for +5v ±0.01v Make this adjustment carefully it is the reference for the delay timing.

(2) With the DELAY MULT. SOURCE switch on INT, and the DELAY MULTIPLIER set to 0.50, check the voltage at pin 9 of the buffer board socket, J104. Voltage must be between 0.25v and 0.27v. If this voltage is incorrect, select R4 on the buffer board. If R4 is changed, repeat step (1).

(3) With the MULT. SOURCE switch on EXT and the DELAY ANALOG IN connector (J304) grounded, measure the voltage at the DELAY ANALOG OUT connector (J302). Adjust R13, "zero", on the buffer board for 0v. Final adjustment should be made with the meter on a current scale that is capable of resolving 10 μa.

(4) With the MULT. SOURCE switch on INT, and the DELAY MULTIPLIER set to 10.00, measure the voltage at the DELAY ANALOG OUT connector, J303. This output has a source impedance of 1 kΩ which must be considered if the impedance of the measurement device is less than 1 MΩ. The output voltage should be +10v ±2%.

e. Adjust incremental delay range accuracy.

(1) Use the test set-up shown in Fig. 4-2. Trigger the Model 153 with the 1 msec markers. Calibrate the horizontal input of the test oscilloscope with the DELAY MULT. SOURCE switch on INT. Set the DELAY MULTIPLIER to 1.00 and adjust the horizontal positioning so the spot is 1 cm from the left edge of the graticule. Set the DELAY MULTIPLIER to 10.00 and adjust the horizontal input sensitivity so the dot is 10 cm from the left edge of the graticule. Repeat these two adjustments until there is no further interaction.

With the test scope in the external-horizontal input mode, free-run the sweep at 100 msec/cm (1 sec total sweep time) and select the resistor between the sawtooth output and the DELAY ANALOG IN for 10.5 cm of horizontal deflection (approximately 30 kΩ).

Make the above test set-up carefully. It is desirable to read the horizontal axis of the oscilloscope display to better than 1%.

(2) Display the 0.1 μs markers on the 1 μs DELAY RANGE. Adjust the horizontal positioning of the test oscilloscope and R16, "scale", on the buffer board so the last 9 markers coincide with major graticule marks on the test oscilloscope. Check the 10 μs range using 1 μs markers, and the 100 μs range using 10 μs markers in the same fashion. Compromise the adjustment of R16, "scale", for best accuracy of all three ranges. "Worst case" range should be within 2%.

(3) Display a 10 MHz sine wave on the 100 ns delay range, and adjust C19 on the trigger board so the last 9 cycles coincide with the major graticule marks within 1%.

(4) After adjusting the horizontal positioning of the test oscilloscope so each marker coincides with major graticule marks, switch the DELAY MULT. SOURCE switch to INT. Set the DELAY MULTIPLIER to the peak of the marker which is 1 cm from the left

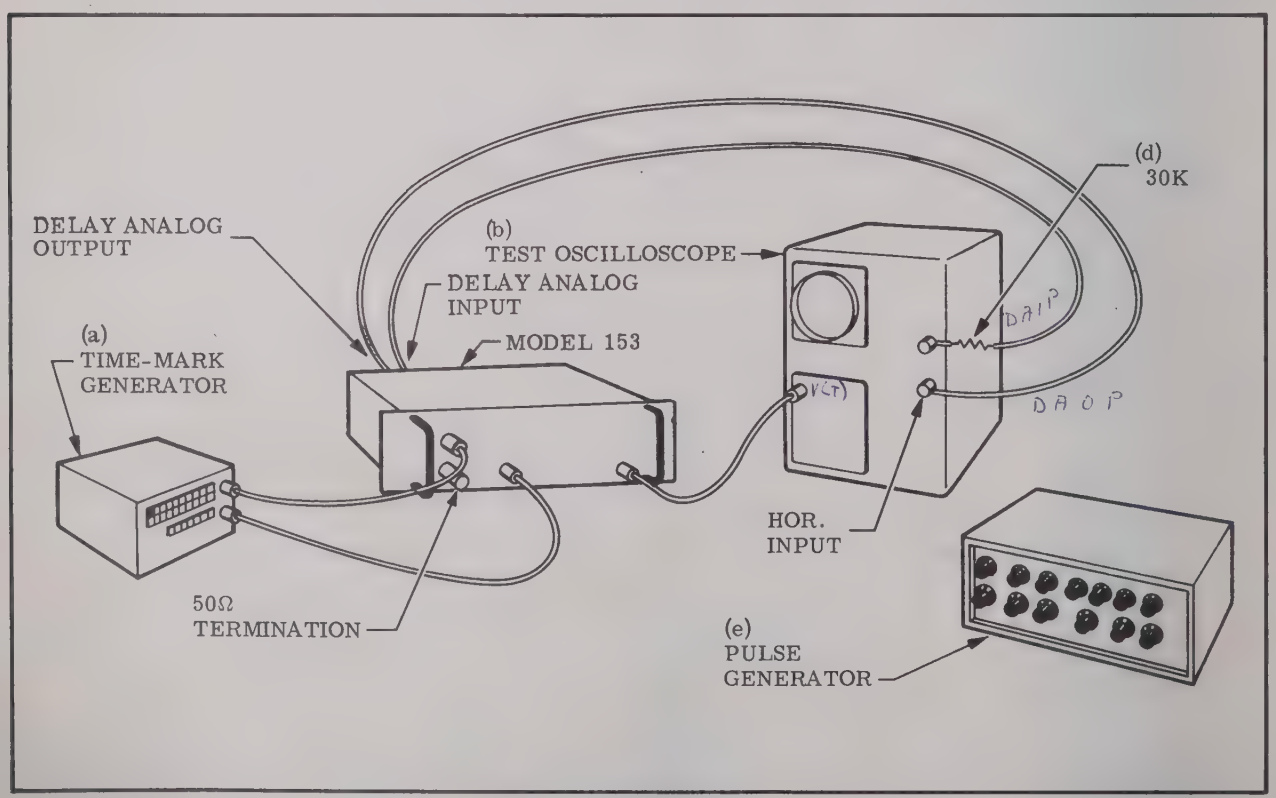


Fig. 4-2 Basic Test Setup

edge of the graticule and then to the peak of the marker which is 10 cm from the left edge of the graticule. The difference between the two settings must be between 8.91 and 9.09.

(5) Repeat step (4) on each of the other 3 DELAY RANGES, using 1/10th full scale markers on each range. On the 1 μs, 10 μs, and 100 μs ranges, the difference between the two settings must be between 8.82 and 9.18.

f. Adjust delay range offset.

(1) With the test set-up described in c. above, display the 20 MHz sine wave (50 ns) on the 100 ns delay range. Check the horizontal calibration of the test oscilloscope; that is, the spot under the 1 cm graticule mark when the DELAY MULTIPLIER is set to 1.00 and under the 10 cm mark when the DELAY MULTIPLIER is set to 10.00.

With the DELAY MULT. SOURCE on EXT, observe the point on the 20 MHz sine wave at the 10 cm graticule mark. Switch to the 1 μs DELAY RANGE, and adjust R20, "offset", on the buffer board so the same point on the 20 MHz sine wave coincides with the 1 cm graticule mark. Switch back and forth between the 100 ns DELAY RANGE and the 1 μs DELAY RANGE while making the adjustment.

Display the 0.5 μs markers using the 1 μs and the 10 μs DELAY RANGES as stated above.

Display the 5 μs markers using the 10 μs and the 100 μs DELAY RANGES as above. Adjust R20, "offset", for the best compromise among all ranges.

g. Internal Waveforms.

(1) Trigger the Model 153 and the test oscilloscope with the 1 msec trigger output from the time-mark generator.

(2) Display the waveform at pin 22 of the trigger board socket, J103, on a 200 ns/cm sweep. Adjust R50, "period", on the trigger board for 200 ns between the negative and the positive spikes which represent the leading and trailing edges of the delayed pulse.

(3) Adjust R56, "period", on the stretcher board for 1.2 μs between the positive spike and the reflection from the trailing edge of the memory gate.

(4) Switch the test oscilloscope to the 1 μs/cm sweep speed and observe the position of strobe time (the negative pulse at pin 22, J103). Without distrubing the test scope, observe the waveform at pin 20 of the stretcher board socket, J102. The waveform should not be less than 0.5 μs wide, approximately 4 μs after strobe time. → 1.2 to 2.2 usec Wide.

h. Adjust transfer characteristics.

(1) Without triggering, and with no signal input, adjust R23, "balance", on the sampler board for equal + and - bias voltage on the sampling bridge. The bridge bias voltages may be measured at the terminals of T1 on the sampler board. The + and - bias voltages should be equal in amplitude and between 0.88v and 0.95v.

(2) Trigger the test oscilloscope and the Model 153 with the 1 ms trigger output from the time-mark generator. Terminate the SIGNAL IN and the SIGNAL OUT connectors on the Model 153, but do not apply an input signal.

Display the output of the sampler board, pin 16 of J101, at 1 μs/cm. Preset the rear-mounted ZERO control to mid-range, and adjust R38, "zero", on the sampler board for 0v output just before the memory gate closes (1.4 μs after strobe time). The output voltage must be within 10 mv of ground before the memory gate terminates. — 4.mV VTout

(3) Set OUTPUT GAIN to X10. With a voltmeter monitor the voltage at the output connector, V(t). Adjust R22, "zero (1)", on the stretcher board for 0v output. Final adjustment should be made on a current scale that can resolve 1 μamp.

(4) Set OUTPUT GAIN to X100. Monitor the voltage at the output connector, V(t). Adjust R37, "zero (2)", on the stretcher board for 0v ±10 mv. Final adjustment should be made on a current scale that can resolve 1 μamp.

(5) Set OUTPUT GAIN to X1. Monitor the output voltage at V(t). Remove the trigger. The output voltage should remain within ±20 mv (±20 μamp if the output is being monitored with a μammeter.

(6) Trigger the Model 153 at 1 kHz. Connect an open 50Ω cable, not less than 2 ns in length, to the SIGNAL OUT connector. Connect the SIGNAL IN connector to the OFFSET INPUT connector. Set OUTPUT GAIN to X1 and alternately apply +1v and -1v to the OFFSET INPUT, and adjust R36, "gain" on the sampler board, for less than 4 mv output at V(t). The +1v and -1v can be accomplished by connecting a 1.5 k resistor between the paralleled inputs and the + or - 15v supplies.

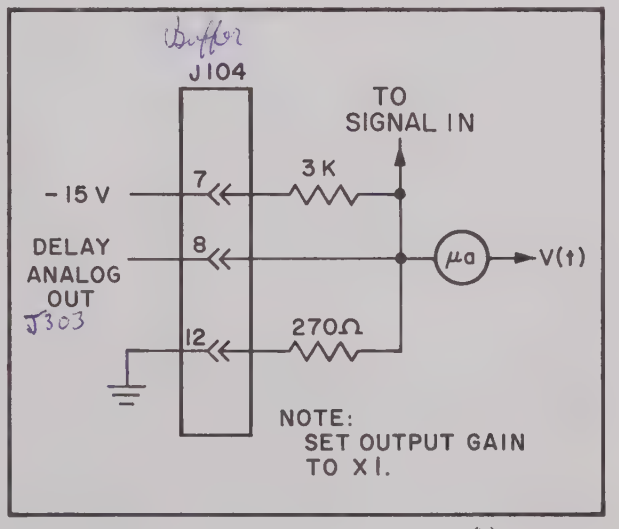


Fig. 4-3 Test set-up for step h. (7)

(7) Pad the output of the delay analog buffer as shown in Fig. 4-3. Set the DELAY MULT. SOURCE to INT, OUTPUT GAIN to X1, remove terminations from the SIGNAL IN and SIGNAL OUT connectors, and trigger the Model 153 at 1 kHz. Adjust R20, "gain", on the stretcher board for minimum reading on the meter through the full range of the DELAY MULTIPLIER control. Maximum reading on the test meter

at any setting of the DELAY MULTIPLIER control should be less than 10 μamp.

i. D/A calibration (if D/A card is installed).

(1) Remove the counter card. Set DELAY MULT. SOURCE to D/A. Monitor the voltage output at the DELAY ANALOG OUT connector, J303. Adjust R12, "zero adjust", on the D/A board for 0v output.

(2) Replace the counter card. Display a 2 MHz sine wave (50 ns) on the 1 μs delay range, using the test set-up shown in Fig. 4-2. Set the DELAY MULTIPLIER to 10.00. Switch the DELAY MULT. SOURCE alternately from D/A to INT. Adjust R15, "scale factor", on the D/A board so the maximum delay from the D/A board is equal to the INT delay.

(3) Repeat steps (1) and (2) until there is no further interaction.

j. Trigger adjustment

(1) Connect the test oscilloscope as shown in Fig. 4-2. Drive the SIGNAL IN from a variable-amplitude 50Ω pulse generator. Connect the SIGNAL OUT to the TRIGGER IN. Set TRIGGER SENSITIVITY fully counter-clockwise. Adjust the amplitude of the pulse generator and determine the minimum amplitude for triggering. Adjust R65, "trigger sensitivity", on the trigger board for a triggering threshold between 90 mv and 100 mv.

SECTION 5
PARTS LIST

5-1 ORDERING INFORMATION

Replacement parts may be ordered through your E-H Representative or from the factory. To be certain that you receive the proper replacement parts, always include the following information with your order:

a. Model number and serial number of the instrument on which the replacement parts will be installed.

b. Circuit or drawing reference for which each part is intended.

c. E-H part number.

For factory repair of this instrument, or warranty claim, contact E-H Research Laboratories, Inc., Customer Service Department, and provide:

(1) Instrument model number and serial number.
(2) Full details concerning the nature of the malfunction.

Individual components in this instrument that are identified by a 6-digit E-H part number may be replaced with parts of like value and quality providing the replacement part is the same physical size and has the same value and tolerances specified in the parts list. Components identified with a 5-digit E-H part number, or marked with an asterisk (*), are factory selected or come in matched sets. Replacements for factory Select parts should be ordered through your E-H Representative or from the factory.

The circuit or drawing reference numbers start with "1" on each etched circuit board. For example; there is an R1 on the Sampler Board, there is also an R1 on the Stretcher Board. It is necessary to include the etched circuit board terminology in the circuit number to distinguish between the two.

Normally, individual wafers or contacts are not supplied for switch repair. If switch repair is necessary, it is more practical to replace the entire switch.

Etched circuit boards are available complete with mounted components. Refer to the following index for E-H part numbers. The individual components on each board are tabulated in the paragraph noted for that board.

INDEX

	E-H Part #s	Paragraph
Sampler	12634	5-2
Stretcher	12637	5-3
Trigger	12640	5-4
Counter	12643	5-5
Buffer	12646	5-6
Regulator	12649	5-7
D/A Converter	12652	5-8
Miscellaneous		5-9

5-2 SAMPLER BOARD

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
C1	Cap., 10pf	311-051
C2	Cap., .001μf	311-016
C3	Cap., 1.0μf, 25v	311-038
C4	Cap., 75pf	311-025
C5	Cap., .002μf	311-017
C6	Cap., 1.0μf, 25v	311-038
C7	Cap., 1.0μf, 25v	311-038
C8	Cap., .01μf	311-012
C9	Cap., .1μf, 50v	311-034
C10	Cap., 25μf, 25v	316-028
C11	Cap., 1.0μf, 25v	311-038
C12	Cap., .1μf, 50v	311-034
C13	Cap., 25μf, 25v	316-028
C14	Cap., 1.0μf, 25v	311-038
CR1A	Diode	11758
CR1B	Diode	11758
CR1C	Diode	11758
CR1D	Diode	11758
CR2	Diode, zener	12529
CR3	Diode, zener	12529
CR4	Diode, zener	12529
CR5	Diode, 1N914B	376-022
CR6	Diode, zener	12529
Q1A	Transistor	663-092
Q1B	Transistor	663-029
Q2	Transistor	11749
Q3A	Transistor	11759
Q3B	Transistor	11759
Q4	Transistor	11749
Q5	Transistor, 2N3251	663-076
Q6	Transistor	11477
Q7	Transistor	11477
Q8	Transistor	11722
Q9	Transistor	11722
Q10	Transistor	11770
Q11	Transistor	11770
Q12	Transistor, 2N3906	663-071
Q13	Transistor	11749
Q14	Transistor, 2N3906	663-071
Q15A	Transistor	11748
Q15B	Transistor	11748
R1	Resistor, 10K, 1/4W, 5%	595-103
R2	Resistor, 5.1M, 1/4W, 5%	595-515
R3	Resistor, 10K, 1/4W, 1%	617-012
R4	Resistor, 2K, 1/4W, 5%	595-202
R5	Resistor, 51Ω, 1/4W, 5%	595-510
R6	Resistor, 4.02K, 1/4W, 1%	617-010
R7	Resistor, 4.02K, 1/4W, 1%	617-010

5-2 SAMPLER BOARD
Continued

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
R8	Resistor, 1.1K, 1.4W, 1%	617-023
R9	Resistor, 1K, 1/4W, 1%	617-002
R10	Resistor, 4.22K, 1/2W, 1%, MF	618-048
R11	Resistor, 10K, 1/4W, 1%	617-012
R12	Resistor, 200Ω, 1W, 5%	597-201
R13	Resistor, 3K, 1/4W, 5%	595-302
R14	Resistor, 1.65K, 1/2W, 1%, MF	618-011
R15	Resistor, 20Ω, 1/4W, 5%	595-200
R16	Resistor, 1K, 1/4W, 1%	617-002
R17	Resistor, 620Ω, 1/2W, 5%	596-621
R18	Resistor, 47Ω, 1/2W, 5%	596-470
R19	Resistor, 15.4K, 1/2W, 1%, MF	618-072
R20	Resistor, 1K, 1/4W, 1%	617-002
R21	Resistor, 1K, 1/4W, 1%	617-002
R22	Resistor, 15K, 1/2W, 1%, MF	618-092
R23	Trimpot, 1K	551-040
R24	Resistor, 100Ω, 1/4W, 5%	595-101
R25	Resistor, 71.5K, 1/4W, 1%	617-031
R26	Resistor, 100Ω, 1/4W, 5%	595-101
R27	Resistor, 10K, 1/4W, 1%	617-012
R28	Resistor, 100K, 1/4W, 1%	617-016
R29	Resistor, 4.99K, 1/4W, 1%	617-011
R30	Resistor, 100K, 1/4W, 1%	617-016
R31	Resistor, 2K, 1/4W, 5%	595-202
R32	Resistor, 316Ω, 1/4W, 1%	617-027
R33	Resistor, 470Ω, 1/2W, 5%	596-471
R34	Resistor, 475Ω, 1/4W, 1%	617-026
R35	Resistor, 1.82K, 1/4W, 1%	617-021
R36	Trimpot, 200Ω	551-039
R37	Resistor, 200K, 1/4W, 1%	617-017
R38	Trimpot, 10K	551-033
R39	Resistor, 750K, 1/2W, 1%, MF	618-019
R40	Resistor, 51Ω, 1/4W, 5%	595-510
R41	Resistor, 51Ω, 1/4W, 5%	595-510
R42	Resistor, 51Ω, 1/4W, 5%	595-510
R43	Resistor, 300Ω, 3W, ww	610-061
R44	Resistor, 51Ω, 1/4W, 5%	595-510
R45	Resistor, 1.5K, 1/4W, 5%	595-152
R46	Resistor, 330Ω, 1/2W 5%	596-331
R47	Resistor, 100Ω, 1/4W, 5%	595-101
R48	Resistor, 51Ω, 1/4W, 5%	595-510
R49	Resistor, 330Ω, 1/2W, 5%	595-331
R50	Resistor, 1/4W, 5%	595-510
R51	Resistor, 470Ω, 1W, 5%	597-471
R52	Resistor, 10Ω, 1/2W, 5%	596-100
R53	Resistor, 200Ω, 1/2W, 5%	596-100
R54	Resistor, 200Ω, 1W, 5%	597-201
T1	Transformer	C 12686
T2	Transformer	C 12687

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
5-3 STRETCHER BOARD		
C1	Cap., .01μf	311-012
C2	Cap., 2500pf, Poly	326-011
C3	Cap., 75pf	311-025
C4	Cap., 50pf	311-006
C5	Cap., 100pf	311-007
C6	Cap., 50pf	311-006
C7	Cap., 200pf	311-028
C8	Cap., 200pf, Poly	326-016
C9	Cap., 20pf	311-002
C10	Cap., 200pf	311-028
C11	Cap., 3900pf, Poly	326-015
C12	Cap., 25μf, 25v	316-028
C13	Cap., .1μf, 50v	311-034
C14	Cap., 25μf, 25v	316-028
C15	Cap., .1μf, 50v	311-034
C16	Cap., .1μf, 50v	311-034
CR1A	Diode, FD777 M Quad	11760
CR1B	Diode, FD777 M Quad	11760
CR1C	Diode, FD777 M Quad	11760
CR1D	Diode, FD777 M Quad	11760
CR2	Diode, zener	374-064
CR3	Diode, FD777	376-059
CR4	Diode, zener	12529
CR5	Deleted	
CR6	Diode, FD777	376-059
CR7	Diode, FD777	376-059
CR8	Diode, zener	12529
CR9A	Diode, zener	11730
CR9B	Diode, zener	11730
CR10	Diode, FD777	376-059
CR11	Diode, FD777	376-059
CR12	Diode, FD777	376-059
CR13	Diode, FD777	376-059
L1	Choke, .68μh	335-013
L2	Choke, 1.02μh	335-022
Q1A	Transistor	663-092
Q1B	Transistor	663-092
Q2	Transistor	11749
Q3A	Transistor, 2N3906 MP	A 11759
Q3B	Transistor, 2N3906 MP	A 11759
Q4	Transistor	11749
Q5	Transistor	11724
Q6	Transistor, 2N3904	663-070
Q7	Transistor, 2N3904	663-070
Q8	Transistor, 2N3906	663-071
Q9	Transistor	11724
Q10	Transistor, 2N3906	663-071
Q11	Transistor, 2N3906	663-071

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
5-3 STRETCHER BOARD Continued		
Q12	Transistor, 2N3906	663-071
Q13	Transistor, 2N3906	663-071
Q14	Transistor	11757
Q15	Transistor	11757
Q16	Transistor, 2N3904	663-070
R1	Resistor, 15.4K, 1/2W, 1%	618-072
R2	Resistor, 15.4K, 1/2W, 1%	618-072
R3	Resistor, 22M, 1/4W, 5%	595-226
R4	Resistor, 22M, 1/4W, 5%	595-226
R5	Resistor, 22M, 1/4W, 5%	595-226
R6	Resistor, 22M, 1/4W, 5%	595-226
R7	Resistor, 22M, 1/4W, 5%	595-226
R8	Resistor, 41.2K, 1/2W, 1%	618-064
R9	Resistor, 41.2K, 1/2W, 1%	618-064
R10	Resistor, 1K, 1/4W, 5%	595-102
R11	Resistor, 10K, 1/4W, 1%	617-012
R12	Resistor, 2K, 1/4W, 5%	595-202
R13	Resistor, 7.5K, 1/4W, 5%	595-752
R14	Resistor, 2.7K, 1/4W, 5%	595-272
R15	Resistor, 3K, 1/4W, 5%	595-302
R16	Resistor, 100Ω, 1/4W, 5%	595-101
R17	Resistor, 2.4K, 1W, 5%	597-242
R18	Resistor, 2K, 1/4W, 1%	617-003
R19	Resistor, 866Ω, 1/2W, 1%	618-067
R20	Trimpot, 200Ω	551-039
R21	Resistor, 402K, 1/4W, 1%	617-018
R22	Trimpot, 20K	551-034
R23	Resistor, 1K, 1/4W, 1%	617-002
R26	Resistor, 1M, 1/4W, 1%	595-105
R27	Resistor, 12K, 1/4W, 5%	595-123
R28	Resistor, 1K, 1/4W, 5%	595-102
R29	Resistor, 12K, 1/4W, 5%	595-123
R30	Resistor, 100Ω, 1/4W, 5%	595-101
R31	Resistor, 10K, 1/4W, 5%	595-103
R32	Resistor, 2K, 1W, 5%	597-202
R33	Resistor, 10K, 1/2W, 1/4%	614-003
R34	Resistor, 1, 11K, 1/2W, 1/4%	614-001
R35	Resistor, 1K, 1/2W, 1%	618-007
R36	Resistor, 511K, 1/2W, 1%	618-013
R37	Trimpot, 20K	551-034
R38	Resistor, 1K, 1/4W, 5%	595-102
R39	Resistor, 680Ω, 1/2W, 5%	596-681
R40	Resistor, 1.5K, 1/4W, 5%	595-152
R41	Resistor, 200Ω, 1/4W, 5%	595-201
R42	Resistor, 30K, 1/4W, 5%	595-303
R43	Resistor, 750Ω, 1/4W, 5%	595-751
R44	Resistor, 1.5K, 1/4W, 5%	595-152
R45	Resistor, 1.5K, 1/4W, 5%	595-152
R46	Resistor, 750Ω, 1/4W, 5%	595-751

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
5-3 STRETCHER BOARD Continued		
R47	Resistor, 10K, 1/4W, 5%	595-103
R48	Resistor, 150K, 1/4W, 5%	595-154
R49	Resistor, 1.8K, 1/4W, 5%	595-182
R50	Resistor, 30K, 1/4W, 5%	595-303
R51	Resistor, 1.5K, 1/4W, 5%	595-152
R52	Resistor, 1.5K, 1/4W, 5%	595-152
R53	Resistor, 560Ω, 1/2W, 5%	596-561
R54	Resistor, 100Ω, 1/4W, 5%	595-101
R55	Resistor, 1K, 1/4W, 5%	595-102
R56	Trimpot, 2K	551-038
R57	Resistor, 1K, 1/2W, 5%	596-102
R58	Resistor, 270Ω, 1/4W, 5%	595-271
R59	Resistor, 3K, 1/4W, 5%	595-302
R60	Resistor, 2K, 1/4W, 5%	595-202
R61	Resistor, 10Ω, 1/2W, 5%	596-100
R62	Resistor, 10Ω, 1/2W, 5%	596-100
R63	Resistor, 10Ω, 1/2W, 5%	596-100
R64	Resistor, 1K, 1/4W, 5%	595-102
T1	Transformer	C 12692
5-4 TRIGGER BOARD		
C1	Cap., 1μf, 50v	311-034
C2	Cap., 1μf, 50v	311-034
C3	Cap., 1μf, Mylar	320-011
C4	Cap., 25pf, Disc.	311-003
C6	Cap., 410pf	311-071
C7	Cap., .001μf	311-010
C8	Cap., .01μf	311-012
C9	Cap., 1000pf, Poly	316-012
C10	Cap., 4230pf, 1%	311-070
C11	Cap., 047μf, 1%	320-040
C12	Cap., .47 μf, 1%	320-041
C13	Cap., 25μf, 25v	316-028
C14	Cap., .1μf, 50v	311-034
C15	Cap., 25μf, 25v	316-028
C16	Cap., .1μf, 50v	311-034
C17	Cap., 15μf, 50v	316-062
C18	Cap., .01μf	311-012
C19	Cap., 7-25pf	332-005
C20	Cap., .001μf	311-010
C21	Cap., 2.2μf, 25v	311-019
CR1	Diode, 1N3719 TD	376-053
CR2	Diode, zener	12529
CR3	Diode	11764
CR4	Diode, 1N3719 TD	376-053
CR5	Diode, zener	374-019
CR6	Diode, zener	12529

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
5-4 TRIGGER BOARD Continued		
CR7	Diode	11764
CR8A	Diode, zener	11761
CR8B	Diode, zener	11761
CR9	Diode, zener, 1N756A	374-064
CR10	Diode	11742
CR11	Diode	11742
CR12	Diode, zener	12529
CR13	Diode	11742
CR14	Diode	11764
CR15A	Diode, zener	11730
CR15B	Diode, zener	11730
CR16	Diode	11764
CR17	Diode	11764
CR18	Diode	11764
CR19	Diode, zener	12529
CR20	Diode	11764
CR21	Diode	11764
CR22	Diode	11764
L1	Choke, .68μh	335-013
L2	Choke, .68μh	335-013
Q1	Transistor, MP 11749	12973
Q2	Transistor, MP 11749	12973
Q3	Transistor	11749
Q4	Transistor	11477
Q5	Transistor	11477
Q6	Transistor	11757
Q7	Transistor	11757
Q8	Transistor	11749
Q9	Transistor	11749
Q10	Transistor	11749
Q11	Transistor	11749
Q12	Transistor	11757
Q13	Transistor	11757
Q14	Transistor, MM709	663-093
Q15	Transistor, 2N3251	663-076
Q16	Transistor	11762
Q17	Transistor	11762
Q18	Transistor	11762
Q19	Transistor	11757
Q20	Transistor	11757
Q21	Transistor	11749
Q22	Transistor	11749
Q23	Transistor	11757
Q24	Transistor	11757
Q25	Transistor	11757
Q26	Transistor	11757
Q27	Transistor, 2N3251	663-076
Q28	Transistor, 2N3904	663-070

5-4 TRIGGER BOARD
Continued

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
R1	Resistor, 510Ω, 1/2W, 5%	596-511
R2	Resistor, 100Ω, 1/4W, 5%	595-101
R3	Resistor, 1.21K, 1/2W, 1%	618-023
R4	Resistor, 20Ω, 1/4W, 5%	595-200
R5	Resistor, 560Ω, 1/4W, 5%	595-561
R6	Resistor, 100Ω, 1/4W, 5%	595-101
R7	Resistor, 390Ω, 1/4W, 5%	595-391
R8	Resistor, 20Ω, 1/4W, 5%	595-200
R9	Resistor, 5.1Ω, 1/4W, 5%	595-051
R10	Resistor, 470Ω, 1/2W, 5%	596-471
R11	Resistor, 100Ω, 1/4W, 5%	595-101
R12	Resistor, 2K, 1/4W, 5%	595-202
R13	Resistor, 1.8K, 1/2W, 5%	596-182
R14	Resistor, 15Ω, 1/4W, 5%	595-150
R15	Resistor, 1K, 1/4W, 5%	595-102
R16	Resistor, 100Ω, 1/4W, 5%	595-101
R17	Resistor, 249Ω, 1/2W, 1%	618-016
R18	Resistor, 1.5K, 1/4W, 5%	595-152
R19	Resistor, 2K, 1/4W, 5%	595-202
R20	Resistor, 240Ω, 1/4W, 5%	595-241
R21	Resistor, 680Ω, 1/2W, 5%	596-681
R22	Resistor, 18Ω, 1/4W, 5%	595-180
R23	Resistor, 1.33K, 1/2W, 1%	618-076
R24	Resistor, 8.2Ω, 1/4W, 5%	595-082
R25	Resistor, 20Ω, 1/4W, 5%	595-200
R26	Resistor, 1K, 1/2W, 1%	618-007
R27	Resistor, 620Ω, 1/4W, 5%	595-621
R28	Resistor, 100Ω, 1/4W, 5%	595-101
R29	Resistor, 1.5K, 1/2W, 5%	596-152
R30	Resistor, 100Ω, 1/4W, 5%	595-101
R31	Resistor, 620Ω, 1/4W, 5%	595-621
R32	Resistor, 360Ω, 1/2W, 5%	596-361
R33	Resistor, 200Ω, 1/4W, 5%	595-201
R34	Resistor, 100Ω, 1/4W, 5%	595-101
R35	Resistor, 1.5K, 1/4W, 5%	595-152
R36	Resistor, 33K, 1/4W, 5%	595-333
R37	Resistor, 10Ω, 1/4W, 5%	595-100
R38	Resistor, 3.6K, 1/2W, 5%	596-362
R39	Resistor, 100Ω, 1/4W, 5%	595-101
R40	Resistor, 820Ω, 1/2W, 5%	596-821
R41	Resistor, 100Ω, 1/4W, 5%	595-101
R42	Resistor, 432Ω, 1/2W, 1%	618-093
R43	Resistor, 100Ω, 1/2W, 1%	618-025
R44	Resistor, 10Ω, 1/4W, 5%	595-100
R45	Resistor, 470Ω, 1/2W, 5%	596-471
R46	Resistor, 200Ω, 1/4W, 5%	595-201
R47	Resistor, 2K, 1/4W, 5%	595-202
R48	Resistor, 3K, 1/4W, 5%	595-302
R49	Resistor, 1K, 1/4W, 5%	595-102

5-4 TRIGGER BOARD
Continued

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
R50	Trimpot, 2K	551-038
R51	Resistor, 560Ω, 1/4W, 5%	595-561
R52	Resistor, 1.5K, 1/4W, 5%	595-152
R53	Resistor, 330Ω, 1/2W, 5%	596-331
R54	Resistor, 1.5K, 1/4W, 5%	595-152
R55	Resistor, 270Ω, 1/4W, 5%	595-271
R56	Resistor, 1K, 1/2W, 5%	596-102
R57	Resistor, 100Ω, 1/4W, 5%	595-101
R58	Resistor, 1.5K, 1/4W, 5%	595-152
R59	Resistor, 100Ω, 1/4W, 5%	595-101
R60	Resistor, 750Ω, 1/2W, 5%	596-751
R61	Resistor, 750Ω, 1/2W, 5%	596-751
R62	Resistor, 750Ω, 1/2W, 5%	596-751
R63	Resistor, 51Ω, 1/4W, 5%	595-510
R64	Resistor, 51Ω, 1/4W, 5%	595-510
R65	Helitrim, 200Ω	551-042
R66	Resistor, 100Ω, 1/4W, 5%	595-101
R67	Resistor, 15Ω, 1/4W, 5%	595-150

5-5 COUNTER BOARD

CR1	Diode	11742
CR2	Diode	11742
CR3	Diode	11742
CR4	Diode	11742
CR5	Diode	11742
CR6	Diode	11742
CR7	Diode	11742
CR8	Diode	11742
CR9	Diode	11742
CR10	Diode	11742
CR11	Diode	11742
CR12	Diode	11742
IC1	Int. Ckt. 824P	665-009
IC2	Int. Ckt. 824P	665-009
IC3	Int. Ckt. 815P	665-007
IC4	Int. Ckt. 815P	665-007
IC5	Int. Ckt. 817P	665-008
IC6	Int. Ckt. 824P	665-009
IC7	Int. Ckt. 815P	665-007
IC8	Int. Ckt. 817P	665-008
IC9	Int. Ckt. 824P	665-009
IC10	Int. Ckt. 890P	665-010
IC11	Int. Ckt. 890P	665-010
IC12	Int. Ckt. 890P	665-010
IC13	Int. Ckt. 890P	665-010
IC14	Int. Ckt. 890P	665-010
IC15	Int. Ckt. 890P	665-010

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
5-5 COUNTER BOARD Continued		
Q1	Transistor, 2N3904	663-070
Q2	Transistor, 2N3904	663-070
Q3	Transistor, 2N3904	663-070
Q4	Transistor, 2N3904	663-070
Q5	Transistor, 2N3904	663-070
Q6	Transistor, 2N3904	663-070
Q7	Transistor, 2N3904	663-070
Q8	Transistor, 2N3904	663-070
Q9	Transistor, 2N3904	663-070
Q10	Transistor, 2N3904	663-070
Q11	Transistor, 2N3904	663-070
Q12	Transistor, 2N3904	663-070
R1	Resistor, 360Ω, 1/4W, 5%	595-361
R2	Resistor, 1.5K, 1/4W, 5%	595-152
R3	Resistor, 360Ω, 1/4W, 5%	595-361
R4	Resistor, 1.5K, 1/4W, 5%	595-152
R5	Resistor, 360Ω, 1/4W, 5%	595-361
R6	Resistor, 1.5K, 1/4W, 5%	595-152
R7	Resistor, 360Ω, 1/4W, 5%	595-361
R8	Resistor, 1.5K, 1/4W, 5%	595-152
R9	Resistor, 360Ω, 1/4W, 5%	595-361
R10	Resistor, 1.5K, 1/4W, 5%	595-152
R11	Resistor, 360Ω, 1/4W, 5%	595-361
R12	Resistor, 1.5K, 1/4W, 5%	595-152
R13	Resistor, 360Ω, 1/4W, 5%	595-361
R14	Resistor, 1.5K, 1/4W, 5%	595-152
R15	Resistor, 360Ω, 1/4W, 5%	595-361
R16	Resistor, 1.5K, 1/4W, 5%	595-152
R17	Resistor, 360Ω, 1/4W, 5%	595-361
R18	Resistor, 1.5K, 1/4W, 5%	595-152
R19	Resistor, 360Ω, 1/4W, 5%	595-361
R20	Resistor, 1.5K, 1/4W, 5%	595-152
R21	Resistor, 360Ω, 1/4W, 5%	595-361
R22	Resistor, 1.5K, 1/4W, 5%	595-152
R23	Resistor, 360Ω, 1/4W, 5%	595-361
R24	Resistor, 1.5K, 1/4W, 5%	595-152
5-6 BUFFER BOARD		
C1	Cap., .005μf, 1kv	311-011
CR1	Diode, zener, 1N753	374-058
Q1	Transistor, 2N3904	663-070
Q2	Transistor, 2N3904	663-070
Q3	Transistor, 2N3251	663-076
Q4	Transistor, 2N3251	663-076
Q5	Transistor, 2N3904	663-070
Q6	Transistor, 2N3906	663-071

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
5-6 BUFFER BOARD Continued		
Q7	Transistor, 2N3904	663-070
Q8	Transistor, 2N3906	663-071
Q9	Transistor, 2N3904	663-070
Q10	Transistor, 2N3906	663-071
R1	Resistor, 1.87K, 1/2W, 1%	618-017
R2	Trimpot, 200Ω	551-039
R3	Resistor, 12K, 1/4W, 5%	595-123
R4	Resistor, 49.9Ω, 1/2W, 1%	618-090
R5	Resistor, 1K, 1/4W, 5%	595-102
R6	Resistor, 536Ω, 1/2W, 1%	618-074
R7	Resistor, 30K, 1/4W, 5%	595-303
R8	Resistor, 12K, 1/4W, 5%	595-123
R9	Resistor, 1K, 1/4W, 5%	595-102
R10	Resistor, 2K, 1/2W, 1%	618-005
R11	Resistor, 2K, 1/2W, 1%	618-005
R12	Resistor, 249K, 1/2W, 1%	618-068
R13	Trimpot, 20K	551-034
R14	Resistor, 3.9K, 1/2W, 5%	596-392
R15	Resistor, 1K, 1/2W, 1%	618-007
R16	Trimpot, 200Ω	551-017
R17	Resistor, 374Ω, 1/2W, 1%	618-028
R18	Resistor, 100Ω, 1/4W, 5%	595-101
R19	Resistor, 1K, 1/4W, 5%	595-102
R20	Trimpot, 2K	551-038
R21	Resistor, 1.8K, 1/4W, 5%	595-182
R22	Resistor, 390Ω, 1/4W, 5%	595-391
R23	Resistor, 3.6K, 1/4W, 5%	595-362
R24	Resistor, 4.3K, 1/4W, 5%	595-432
R25	Resistor, 150K, 1/4W, 5%	595-154
R26	Resistor, 10K, 1/4W, 5%	595-103
R27	Resistor, 390Ω, 1/4W, 5%	595-391
R28	Resistor, 3.6K, 1/4W, 5%	595-362
R29	Resistor, 4.3K, 1/4W, 5%	595-432
R30	Resistor, 150K, 1/4W, 5%	595-154
R31	Resistor, 10K, 1/4W, 5%	595-103
R32	Resistor, 390Ω, 1/4W, 5%	595-391
R33	Resistor, 3.6K, 1/4W, 5%	595-362
R34	Resistor, 4.3K, 1/4W, 5%	595-432
R35	Resistor, 150K, 1/4W, 5%	595-154
R36	Resistor, 10K, 1/4W, 5%	595-103
5-7 POWER SUPPLY REGULATOR		
C1	Cap., 25μf, 25v	316-028
C2	Cap., 100μf, 25v	316-035
C3	Cap., 0.1μf, 50v	311-034
C4	Cap., 25μf, 25v	316-028
C5	Cap., 100μf, 25v	316-035
C6	Cap., 25μf, 25v	316-028

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
5-7 POWER SUPPLY REGULATOR Continued		
C7	Cap., 100μf, 25v	316-035
C8	Cap., 0.1μf, 50v	311-034
C9	Cap., 25μf, 25v	316-028
C10	Cap., 100μf, 25v	316-035
C11	Cap., 100μf, 6v	316-068
CR1	Diode, 1N914B	376-022
CR2	Diode, 1N914B	376-022
CR3	Diode, 1N4005	376-034
CR4	Diode, 1N914B	376-022
CR5	Diode, zener, 1N936A	374-068
CR6	Diode, zener, 1N749A	374-044
Q1	Transistor	A 11724
Q2	Transistor	A 11724
Q3	Transistor	A 11725
Q4	Transistor	A 11725
Q5	Transistor	A 11725
Q6	Transistor	A 11724
Q7	Transistor	A 11724
Q8	Transistor	A 11724
Q9	Transistor	A 11725
Q10	Transistor	A 11725
Q11	Transistor	A 11725
Q12	Transistor	A 11725
Q13	Transistor	A 11724
R1	Resistor, 1K, 1/2W, 5%	596-102
R2	Resistor, 100Ω, 1/2W, 5%	596-101
R3	Resistor, 5.1K, 1/2W, 5%	596-512
R4	Resistor, 1.8K, 1/2W, 5%	596-182
R5	Resistor, 680Ω, 1/2W, 5%	596-681
R6	Potentiometer, 200Ω	551-039
R7	Resistor, 1.3K, 1/2W, 5%	596-132
R8	Resistor, 1K, 1/2W, 5%	596-102
R9	Resistor, 470Ω, 1/2W, 5%	596-471
R10	Resistor, 820Ω, 1/2W, 5%	596-821
R11	Resistor, 5.6K, 1/2W, 5%	596-562
R12	Resistor, 2.43K, 1/2W, 1%	618-045
R13	Resistor, 2.43K, 1/2W, 1%	618-045
R14	Resistor, 33K, 1/2W, 5%	596-333
R15	Resistor, 680Ω, 1/2W, 5%	596-681
R16	Resistor, 1K, 1/2W, 5%	596-102
R17	Resistor, 200Ω, 1/2W, 5%	596-201
R18	Resistor, 1.3K, 1/2W, 5%	596-132
R19	Resistor, 750Ω, 1/2W, 5%	596-751
R20	Potentiometer, 200Ω	551-039
R21	Resistor, 470Ω, 1/2W, 5%	596-471
R22	Resistor, 2.7K, 1/2W, 5%	596-272
R23	Resistor, 1.5K, 1/2W, 5%	596-152
R24	Resistor, 3K, 1/2W, 5%	596-302
R25	Resistor, 120Ω, 1/2W, 5%	596-121
R26	Resistor, 1.5K, 1/2W, 5%	596-152
R27	Resistor, 1K, 1/2W, 1%	618-007
R28	Resistor, 1K, 1/2W, 1%	618-007
R29	Resistor, 510Ω, 1/2W, 1%	596-511
R30	Resistor, 750Ω, 1/2W, 5%	596-551
R31	Resistor, 62Ω, 1/2W, 5%	596-620
R32	Resistor, 2K, 1/2W, 5%	596-202
5-8 D/A CONVERTER BOARD		
C4	Cap., 25μf, 25v, Elec.	316-028
C5	Cap., .001μf, Cer.	311-010
CR2	Diode, zener, 1N753	374-019
Q4	Transistor, 2N1132	663-024
Q5	Transistor, 2N3906	663-071
Q6	Transistor, 2N3904	663-070
Q7	Transistor, 2N3904	663-070
Q8	Transistor, 2N3906	663-071
Q9	Transistor, 2N3904	663-070
Q10	Transistor, 2N3904	663-070
Q11	Transistor, 2N3906	663-071
Q12	Transistor, 2N3904	663-070
Q13	Transistor, 2N3904	663-070
Q14	Transistor, 2N3906	663-071
Q15	Transistor, 2N3904	663-070
Q16	Transistor, 2N3904	664-070
Q17	Transistor, 2N3906	663-071
Q18	Transistor, 2N3904	663-070
Q19	Transistor, 2N3904	663-070
Q20	Transistor, 2N3906	663-071
Q21	Transistor, 2N3904	663-070
Q22	Transistor, 2N3904	663-070
Q23	Transistor, 2N3906	663-071
Q24	Transistor, 2N3904	663-070
Q25	Transistor, 2N3904	663-070
Q26	Transistor, 2N3906	663-071
Q27	Transistor, 2N3904	663-070
Q28	Transistor, 2N3904	663-070
Q29	Transistor, 2N3906	563-071
Q30	Transistor, 2N3904	663-070
Q31	Transistor, 2N3904	663-070
Q32	Transistor, 2N3906	663-071
Q33	Transistor, 2N3904	663-070
Q34	Transistor, 2N3904	663-070
Q35	Transistor, 2N3906	663-071
Q36	Transistor, 2N3904	663-070
Q37	Transistor, 2N3904	663-070

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
5-8 D/A CONVERTER BOARD Continued		
Q38	Transistor, 2N3906	663-071
Q39	Transistor, 2N3904	663-070
Q40	Transistor, 2N3904	663-070
R12	Potentiometer, 10K	551-033
R13	Resistor, 3K, 1/4W, 5%	595-302
R14	Resistor, 200Ω, 3W, ww	610-042
R15	Pot, 50Ω	551-032
R16	Resistor, 50Ω, 3W, ww	610-068
R17	Resistor, 560Ω, 3W, ww	610-007
R18	Resistor, 6.2K, 1/4W, 5%	595-622
R19	Resistor, 150K, 1/4W, 5%	595-154
R21	Resistor, 2K, 1/4W, 5%	595-202
R22	Resistor, 390Ω, 1/4W, 5%	595-202
R23	Resistor, 3K, 1/4W, 5%	595-302
R25	Resistor, 100K, 1/4W, 5%	595-104
R26	Resistor, 499Ω, 1/4W, 1%,MF	617-005
R27	Resistor, 1K, 1/4W, 1%	617-002
R28	Resistor, 2K, 1/4W, 1%	617-003
R29	Resistor, 4.02K, 1/4W, 1%	617-010
R30	Resistor, 4.99K, 1/4W, 1%	617-011
R31	Resistor, 10K, 1/4W, 1%	617-012
R32	Resistor, 20K, 1/4W, 1%	617-013
R33	Resistor, 40.2K, 1/4W, 1%	617-014
R34	Resistor, 49.9K, 1/4W, 1%	617-015
R35	Resistor, 100K, 1/4W, 1%	617-016
R36	Resistor, 200K, 1/4W, 1%	617-017
R37	Resistor, 402K, 1/4W, 1%	617-018
R38	Resistor, 6.2K, 1/4W, 5%	595-622
R39	Resistor, 150K, 1/4W, 5%	595-154
R40	Resistor, 2K, 1/4W, 5%	595-202
R41	Resistor, 390Ω, 1/4W, 5%	595-391
R42	Resistor, 3K, 1/4W, 5%	595-302
R43	Resistor, 100K, 1/4W, 5%	595-104
R44	Resistor, 6.2K, 1/4W, 5%	595-622
R45	Resistor, 150K, 1/4W, 5%	595-154
R46	Resistor, 2K, 1/4W, 5%	595-202
R47	Resistor, 390Ω, 1/4W, 5%	595-391
R48	Resistor, 3K, 1/4W, 5%	595-302
R49	Resistor, 100K, 1/4W, 5%	595-104
R50	Resistor, 6.2K, 1/4W, 5%	595-622
R51	Resistor, 150K, 1/4W, 5%	595-154
R52	Resistor, 2K, 1/4W, 5%	595-202
R53	Resistor, 390Ω, 1/4W, 5%	595-391
R54	Resistor, 3K, 1/4W, 5%	595-302
R55	Resistor, 100K, 1/4W, 5%	595-104
R56	Resistor, 6.2K, 1/4W, 5%	595-622
R57	Resistor, 150K, 1/4W, 5%	595-154
R58	Resistor, 2K, 1/4W, 5%	595-202
R59	Resistor, 390Ω, 1/4W, 5%	595-391

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
5-8 D/A CONVERTER BOARD Continued		
R60	Resistor, 3K, 1/4W, 5%	595-302
R61	Resistor, 100K, 1/4W, 5%	595-104
R62	Resistor, 6.2K, 1/4W, 5%	595-622
R63	Resistor, 150K, 1/4W, 5%	595-154
R64	Resistor, 2K, 1/4W, 5%	595-202
R65	Resistor, 390Ω, 1/4W, 5%	595-391
R66	Resistor, 3K, 1/4W, 5%	595-302
R67	Resistor, 100K, 1/4W, 5%	595-104
R68	Resistor, 6.2K, 1/4W, 5%	595-622
R69	Resistor, 150K, 1/4W, 5%	595-154
R70	Resistor, 2K, 1/4W, 5%	595-202
R71	Resistor, 390Ω, 1/4W, 5%	595-391
R72	Resistor, 3K, 1/4W, 5%	595-302
R73	Resistor, 100K, 1/4W, 5%	595-104
R74	Resistor, 6.2K, 1/4W, 5%	595-622
R75	Resistor, 150K, 1/4W, 5%	595-154
R76	Resistor, 2K, 1/4W, 5%	595-202
R77	Resistor, 390Ω, 1/4W, 5%	595-391
R78	Resistor, 3K, 1/4W, 5%	595-302
R79	Resistor, 100K, 1/4W, 5%	595-104
R80	Resistor, 6.2K, 1/4W, 5%	595-622
R81	Resistor, 150K, 1/4W, 5%	595-154
R82	Resistor, 2K, 1/4W, 5%	595-202
R83	Resistor, 390Ω, 1/4W, 5%	595-391
R84	Resistor, 3K, 1/4W, 5%	595-302
R85	Resistor, 100K, 1/4W, 5%	595-104
R86	Resistor, 6.2K, 1/4W, 5%	595-622
R87	Resistor, 150K, 1/4W, 5%	595-154
R88	Resistor, 2K, 1/4W, 5%	595-202
R89	Resistor, 390Ω, 1/4W, 5%	595-391
R90	Resistor, 3K, 1/4W, 5%	595-302
R91	Resistor, 100K, 1/4W, 5%	595-104
R92	Resistor, 6.2K, 1/4W, 5%	595-622
R93	Resistor, 2K, 1/4W, 5%	595-154
R94	Resistor, 2K, 1/4W, 5%	595-202
R95	Resistor, 390Ω, 1/4W, 5%	595-391
R96	Resistor, 3K, 1/4W, 5%	595-302
R97	Resistor, 100K, 1/4W, 5%	595-104
R98	Resistor, 6.2K, 1/4W, 5%	595-622
R99	Resistor, 150K, 1/4W, 5%	595-154
R100	Resistor, 2K, 1/4W, 5%	595-202
R101	Resistor, 390Ω, 1/4W, 5%	595-391
R102	Resistor, 3K, 1/4W, 5%	595-302
R103	Resistor, 100K, 1/4W, 5%	595-104
5-9 MISCELLANEOUS		
C101	Cap., 1500μf, 50v	316-045

5-9 MISCELLANEOUS
Continued

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
C102	Cap., 1500μf, 50v	316-045
C103	Cap., 1500μf, 50v	316-045
C104	Cap., 1500μf, 50v	316-045
C105	Cap., 1500μf, 50v	316-045
C106	Cap., 1500μf, 50v	316-045
C107	Cap., 4000μf, 15v	316-003
CR101	Diode, 1N4005	376-034
CR102	Diode, 1N4005	376-034
CR103	Diode, 1N4005	376-034
CR104	Diode, 1N4005	376-034
CR105	Diode, 1N4720	376-062
CR106	Diode, 1N4720	376-062
CR107	Diode, 1N4720	376-062
CR108	Diode, 1N4720	376-062
CR109	Diode, 1N4005	376-034
CR110	Diode, 1N4005	376-034
CR111	Diode, 1N4005	376-034
CR112	Diode, 1N4005	376-034
Q101	Transistor, 2N3767	663-085
Q102	Transistor, 2N3767	663-085
Q103	Transistor	11705
Q104	Transistor	11705
Q105	Transistor	11705
R101	Resistor, 2.7Ω, 1/2W, 5%	596-027
R102	Resistor, 2.7Ω, 1/2W, 5%	596-027

5-9 MISCELLANEOUS
Continued

CIRCUIT REFERENCE	DESCRIPTION	E-H PART NO.
R103	Resistor, 50Ω, 3W	610-068
R104	Resistor, 50Ω, 3W	610-068
R105	Resistor, 1Ω, 3W	610-069
R106	Resistor, 1Ω, 3W	610-069
R107	Resistor, 3Ω, 3W	610-048
R108	Resistor, 10Ω, 5W	610-099
R109	Resistor, 1Ω, 3W	610-069
R110	Resistor, 100K, 1/2W, 5%	596-104
R201	Resistor, 8.89K, 1/2W, 1/4%, MF	614-002
R202	Resistor, 1.11K, 1/2W, 1/4%, MF	614-001
R203	Helipot, 1K, 10T	540-010
R204	Dual Potentiometer Bridged	550-037
R205	Resistor, 51Ω, 1/2W, 5%	596-510
R206	Resistor, 51Ω, 1/2W, 5%	596-510
R207	Resistor, 1K, 1/4W, 5%	595-102
R301	Potentiometer, 10K, 2W	545-006
S201	POWER (Toggle)	630-006
S202	OUTPUT GAIN (Rotary)	
S203	TRIGGER POLARITY (Toggle)	630-013
S204	DELAY RANGE (Rotary)	624-055
S205	DELAY MULTI. SOURCE (Rotary)	
T101	Power Transformer	10618
T201	Core, 3E2A	361-011

SECTION 6
DRAWINGS

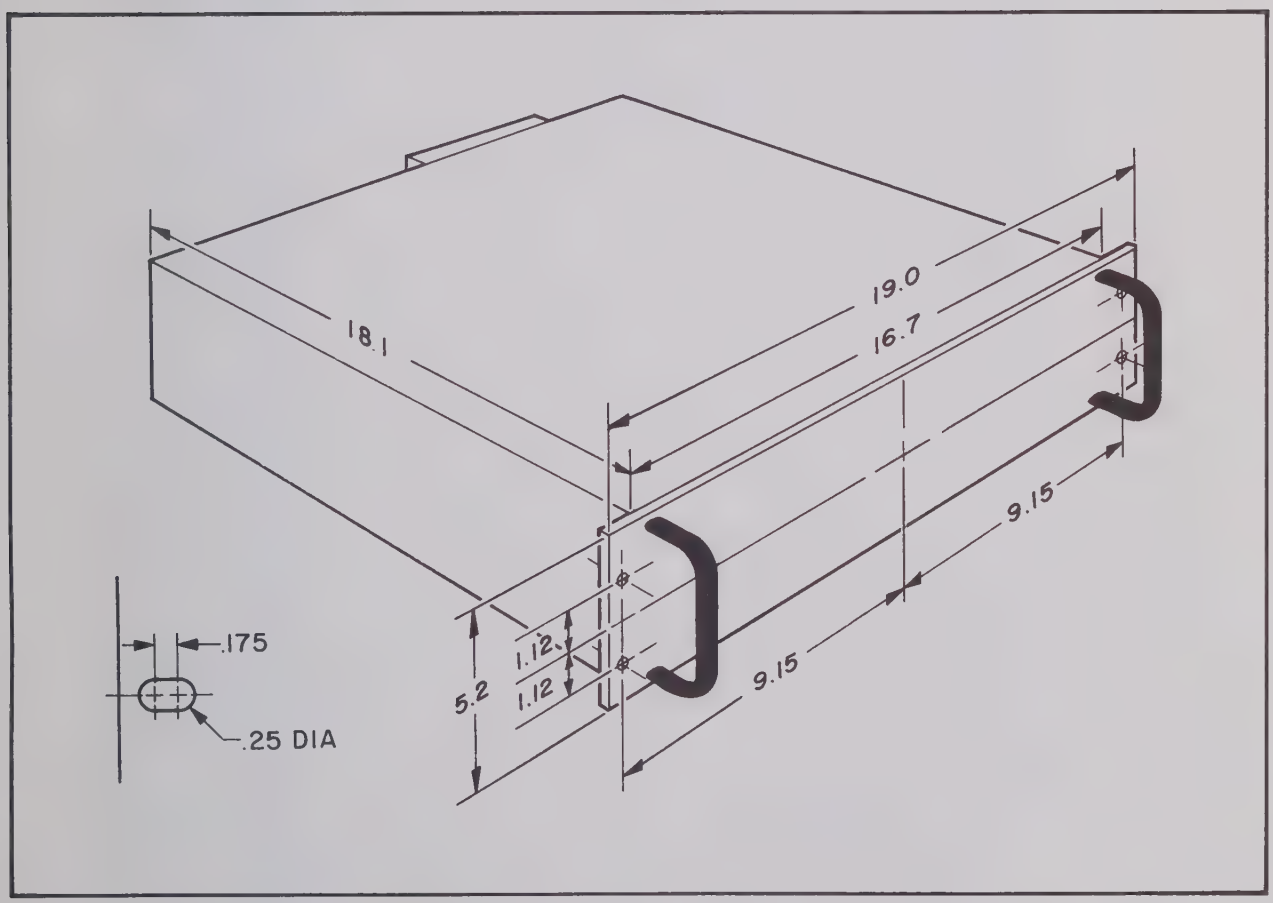


Fig. 6-1 Outline Dimensions

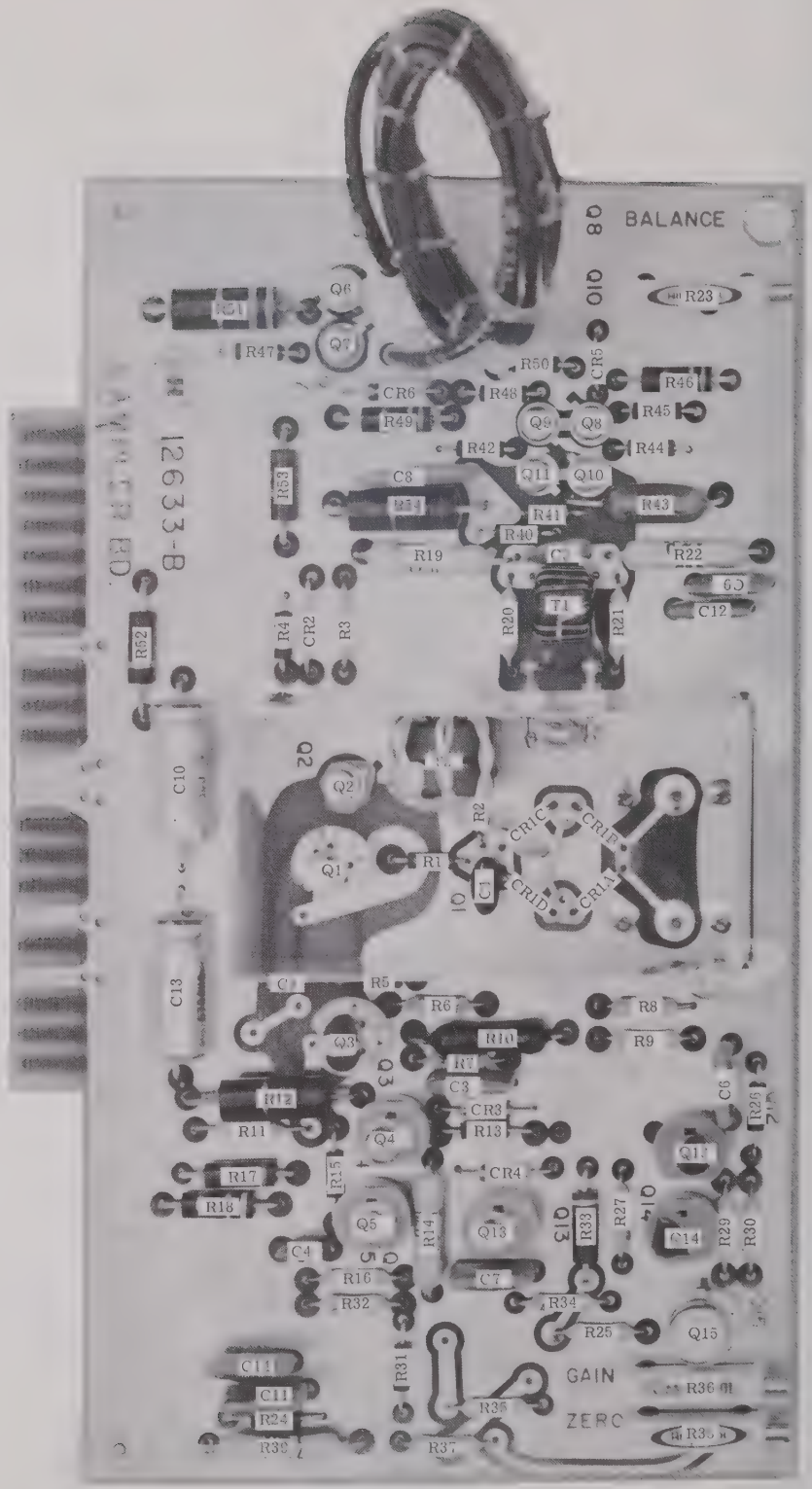


Fig. 6-2 Sampler Board 12634

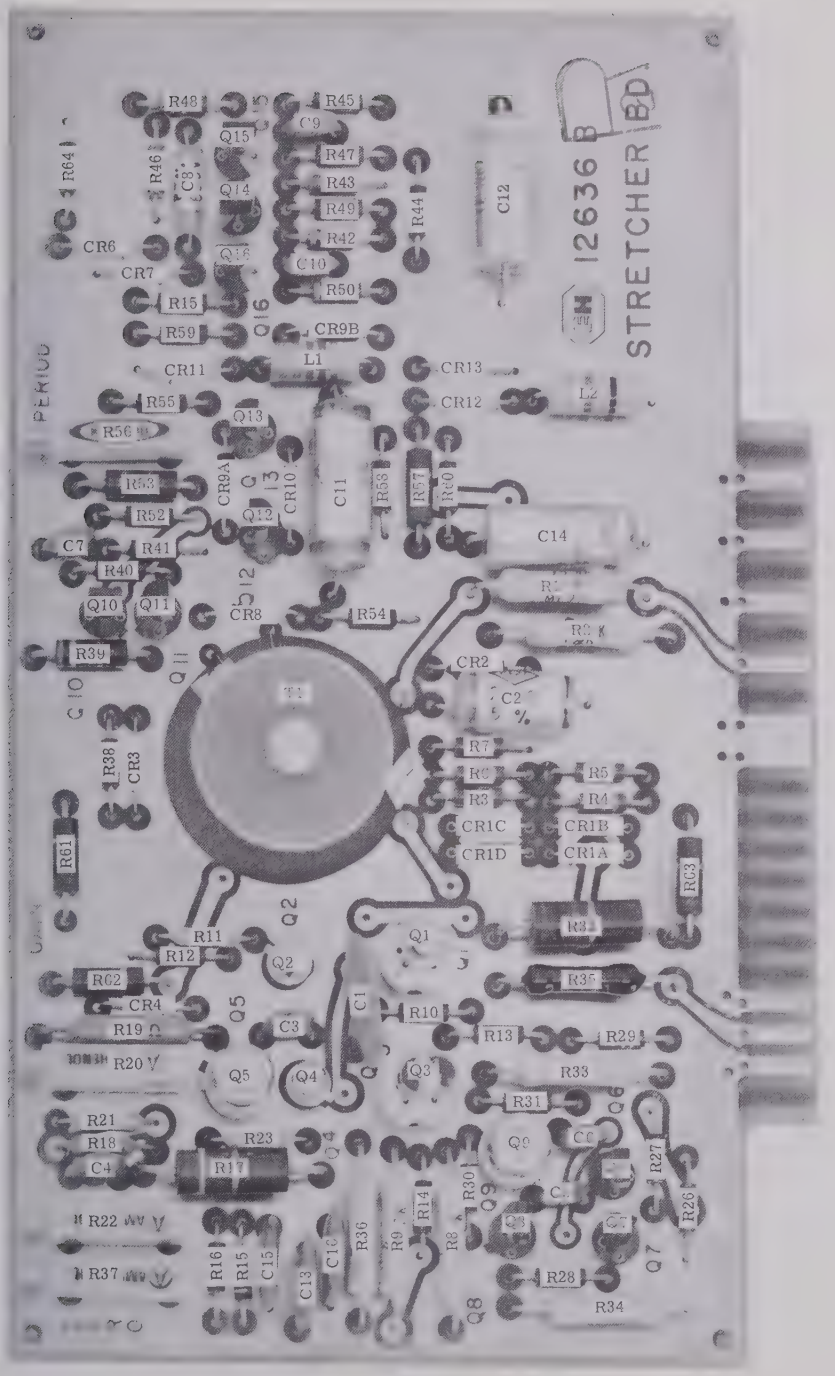


Fig. 6-3 Stretcher Board 12637

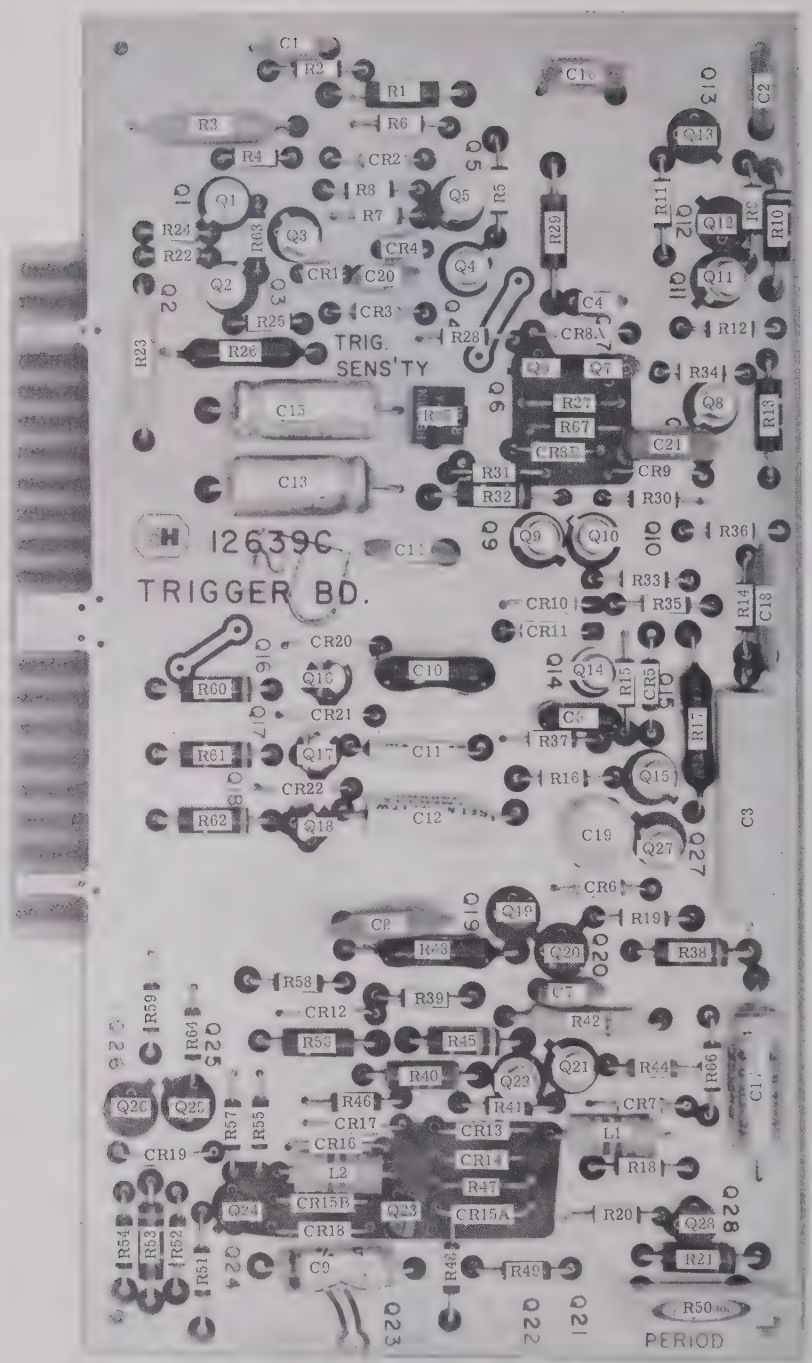


Fig. 6-4 Trigger Board 12640

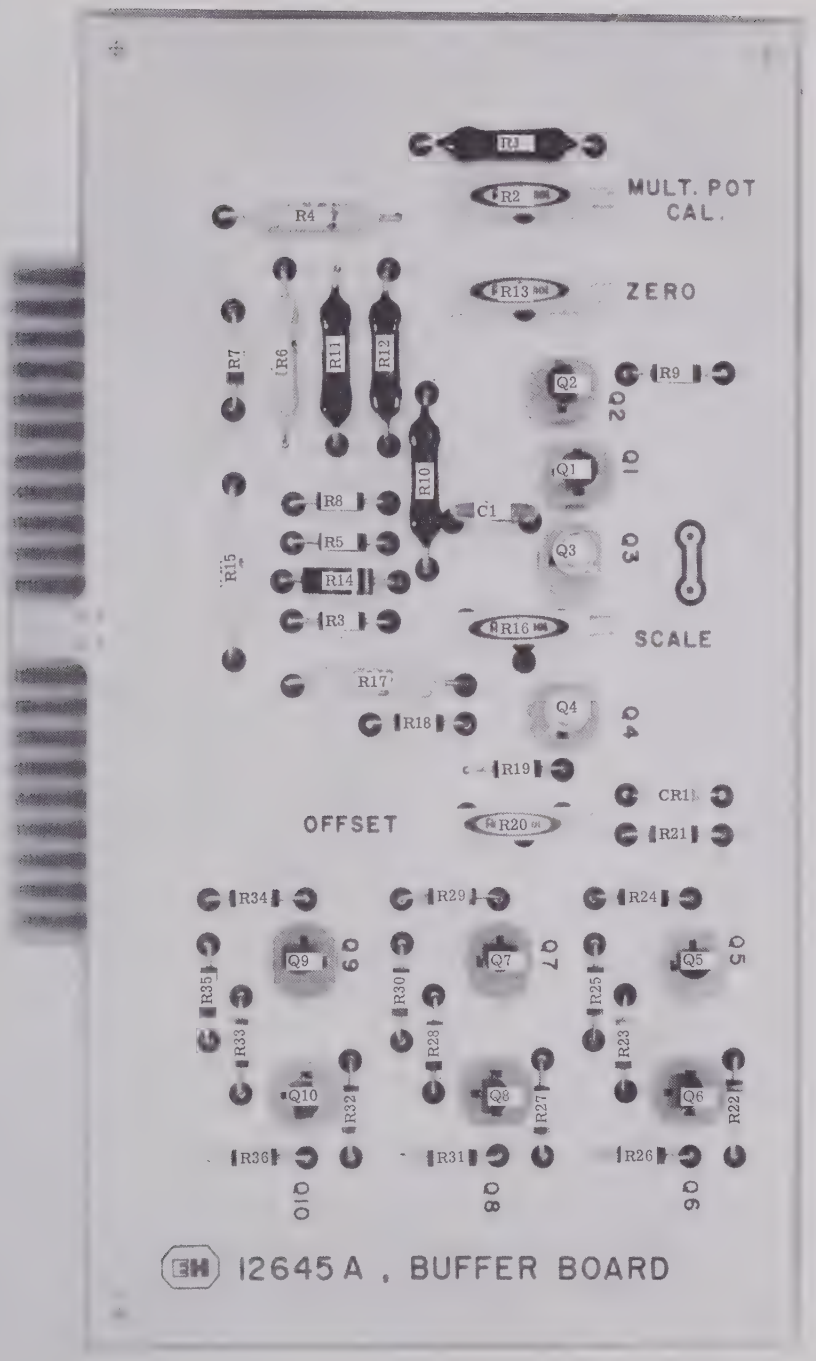


Fig. 6-5 Buffer Board 12646

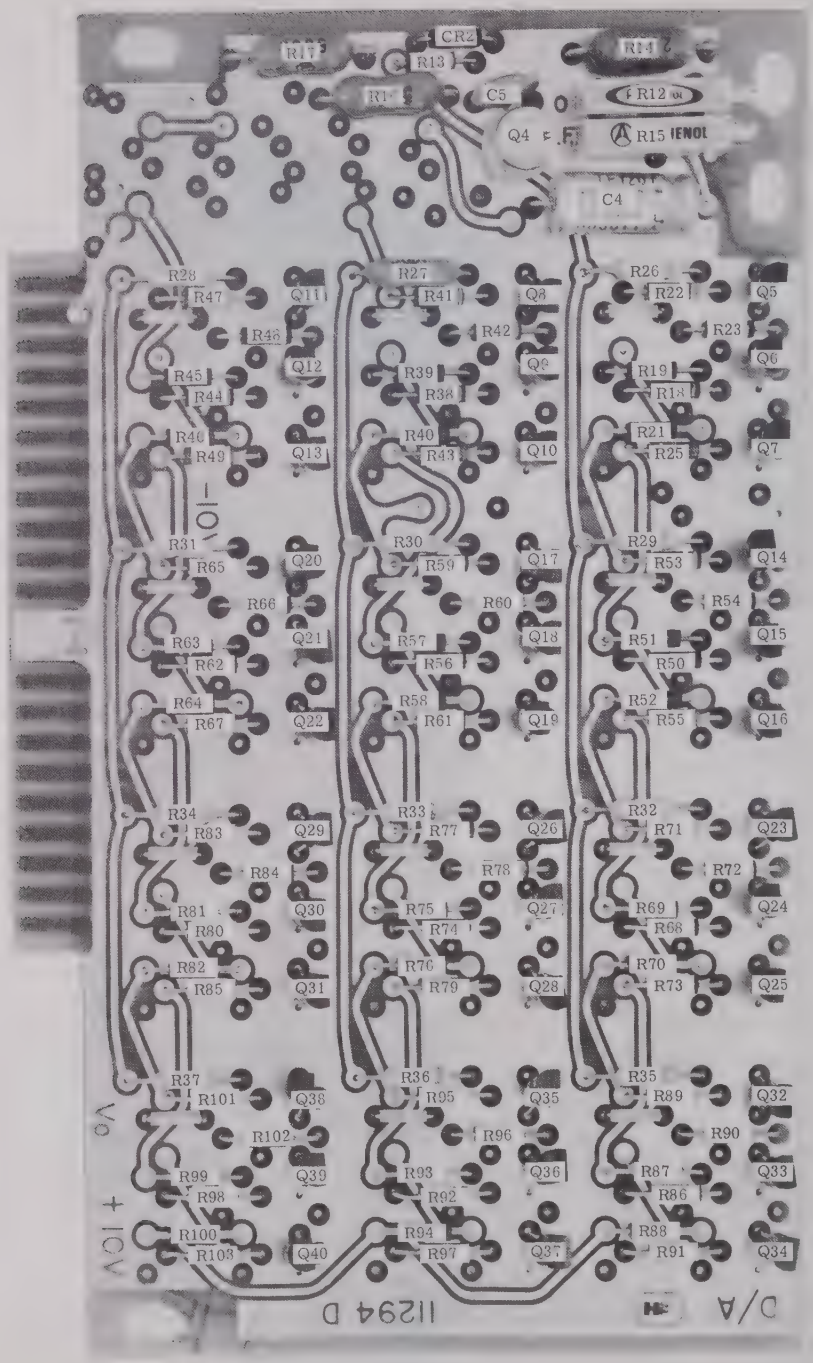


Fig. 6-6 D/A Converter Board 12652

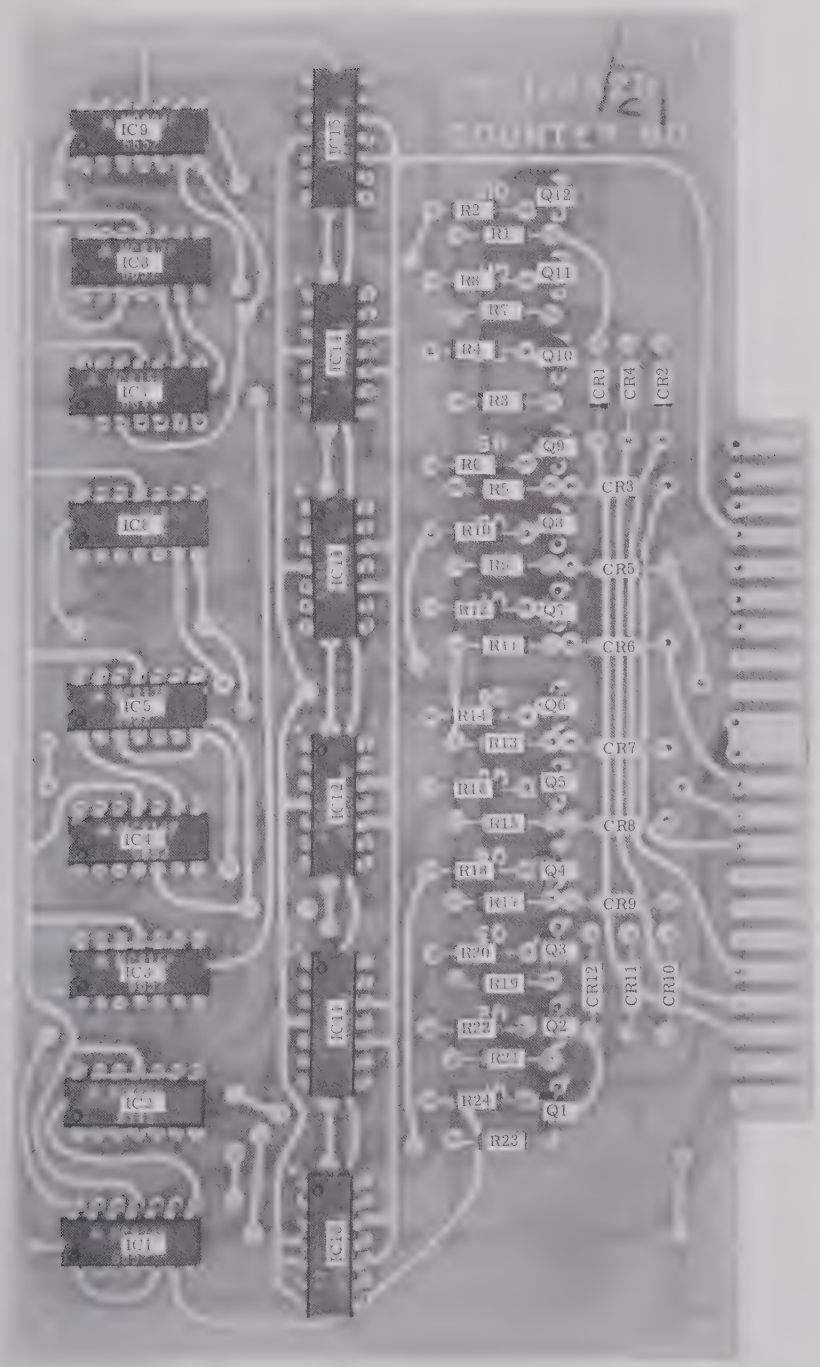
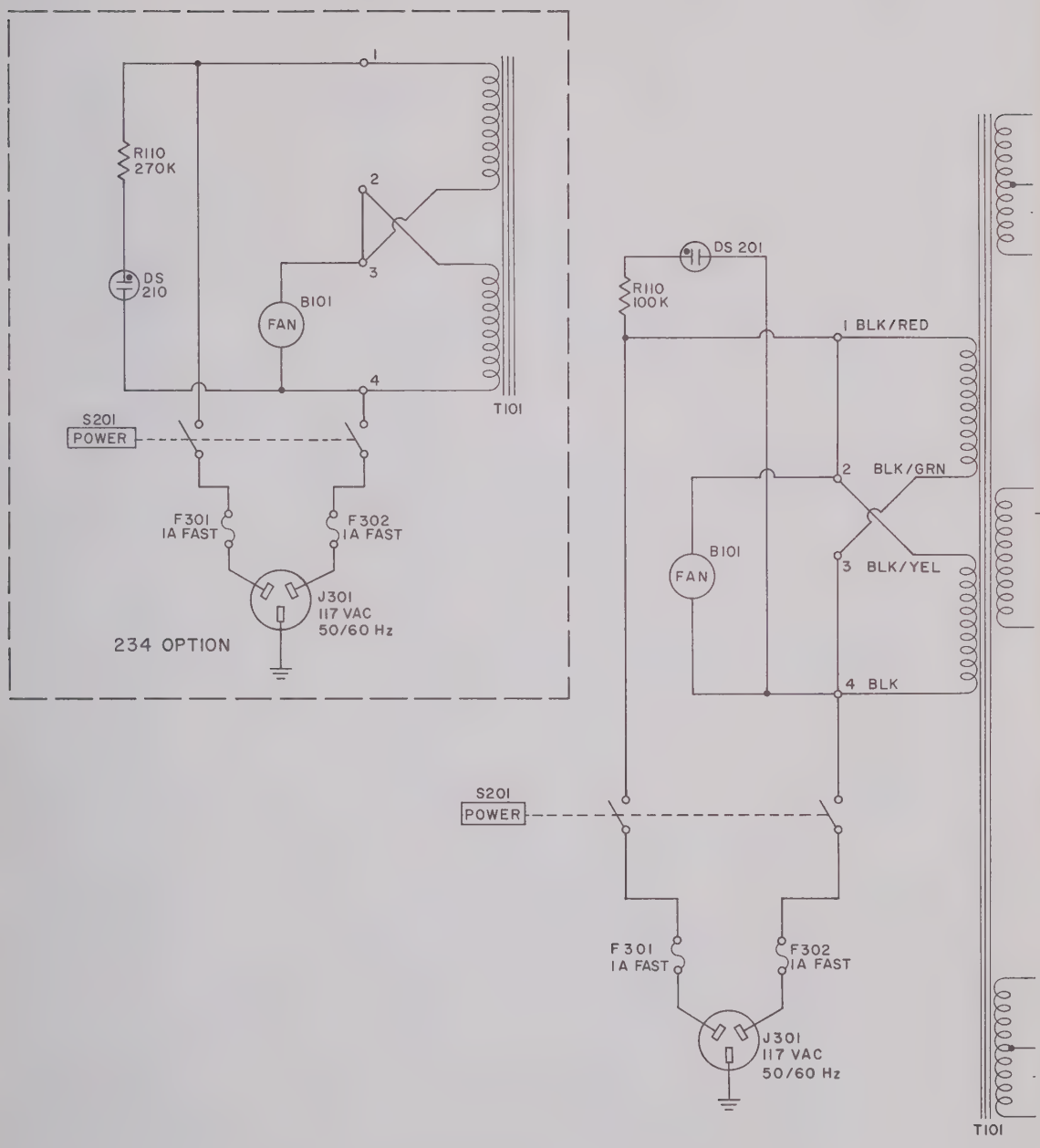
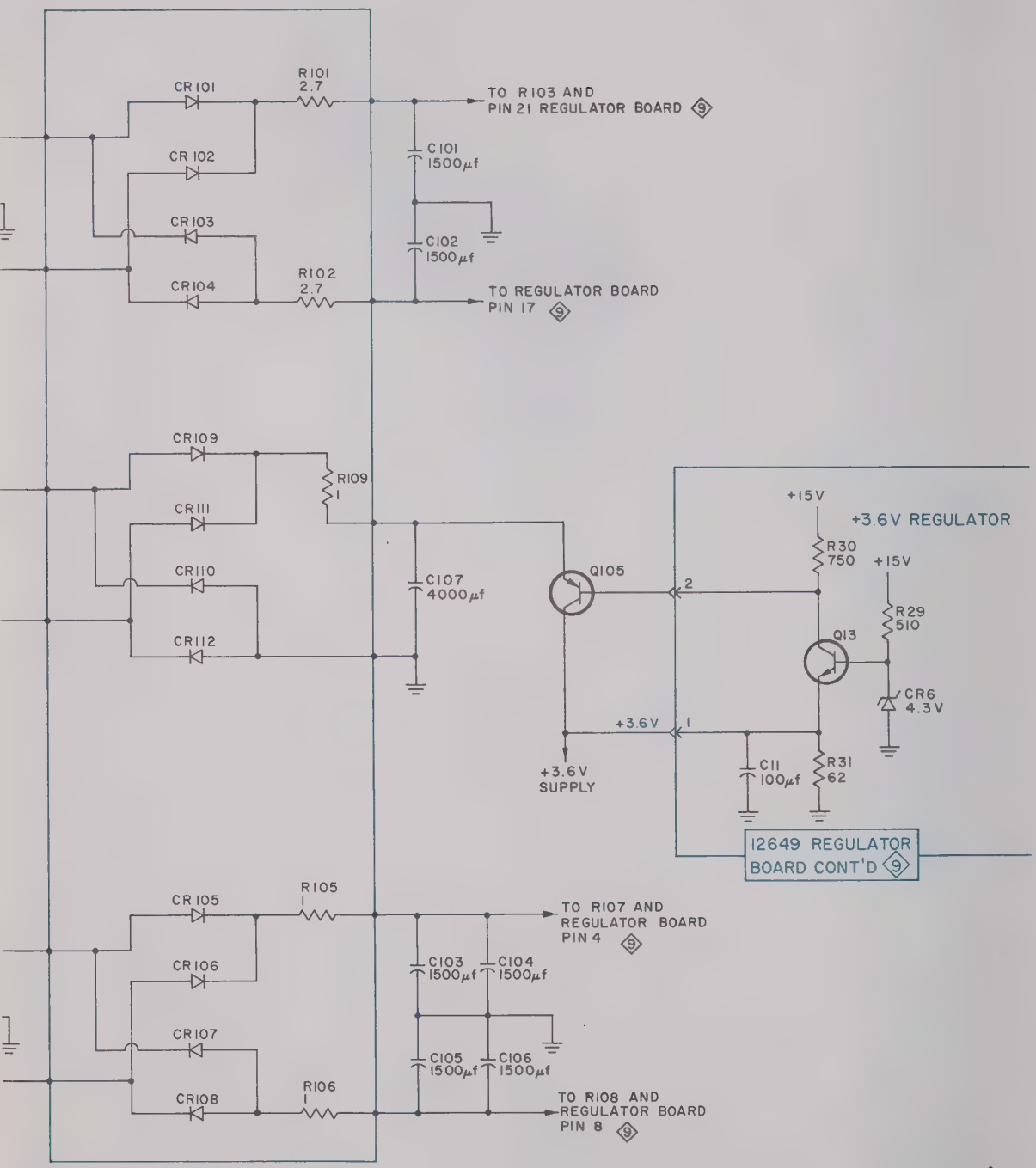
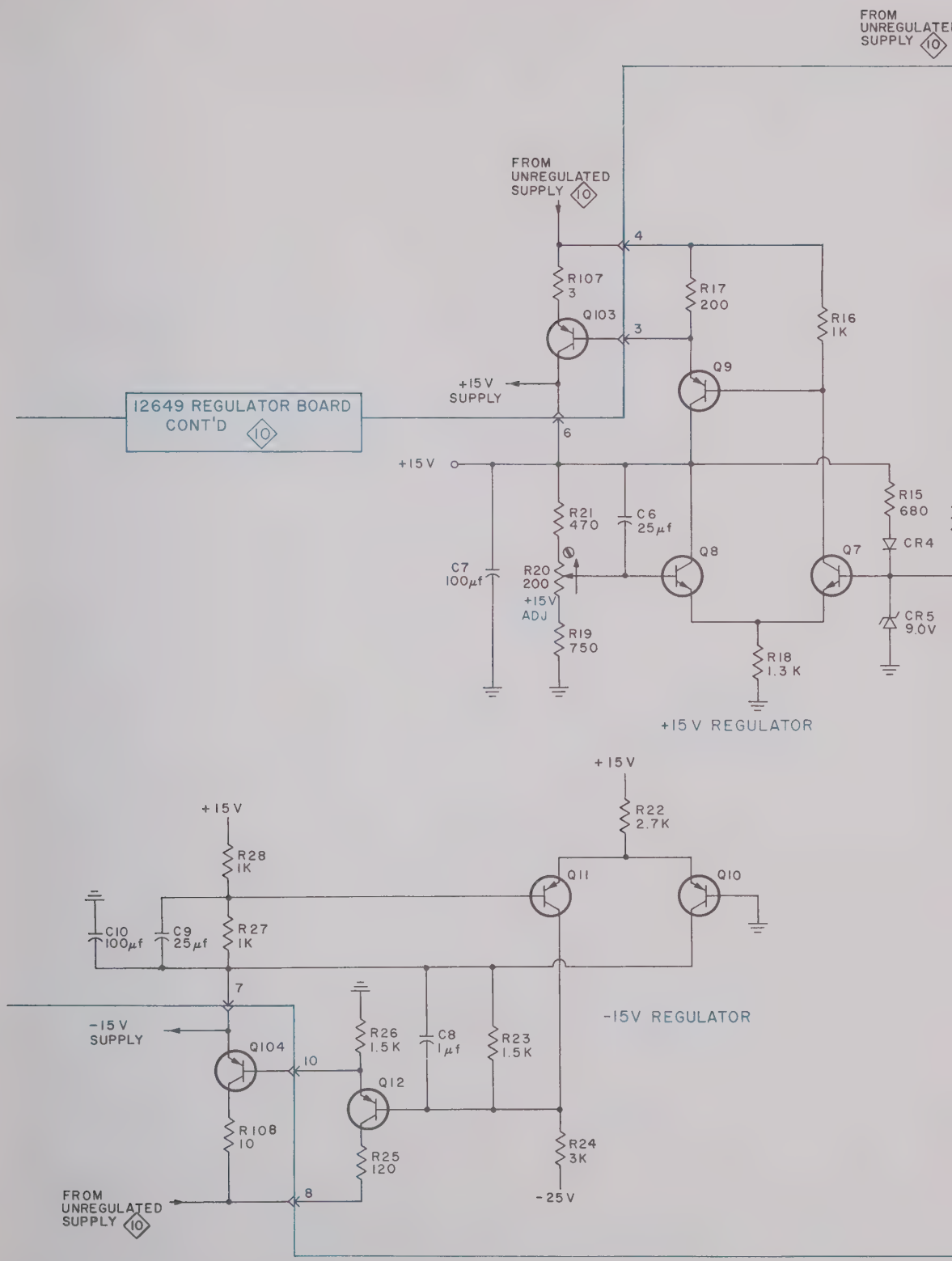
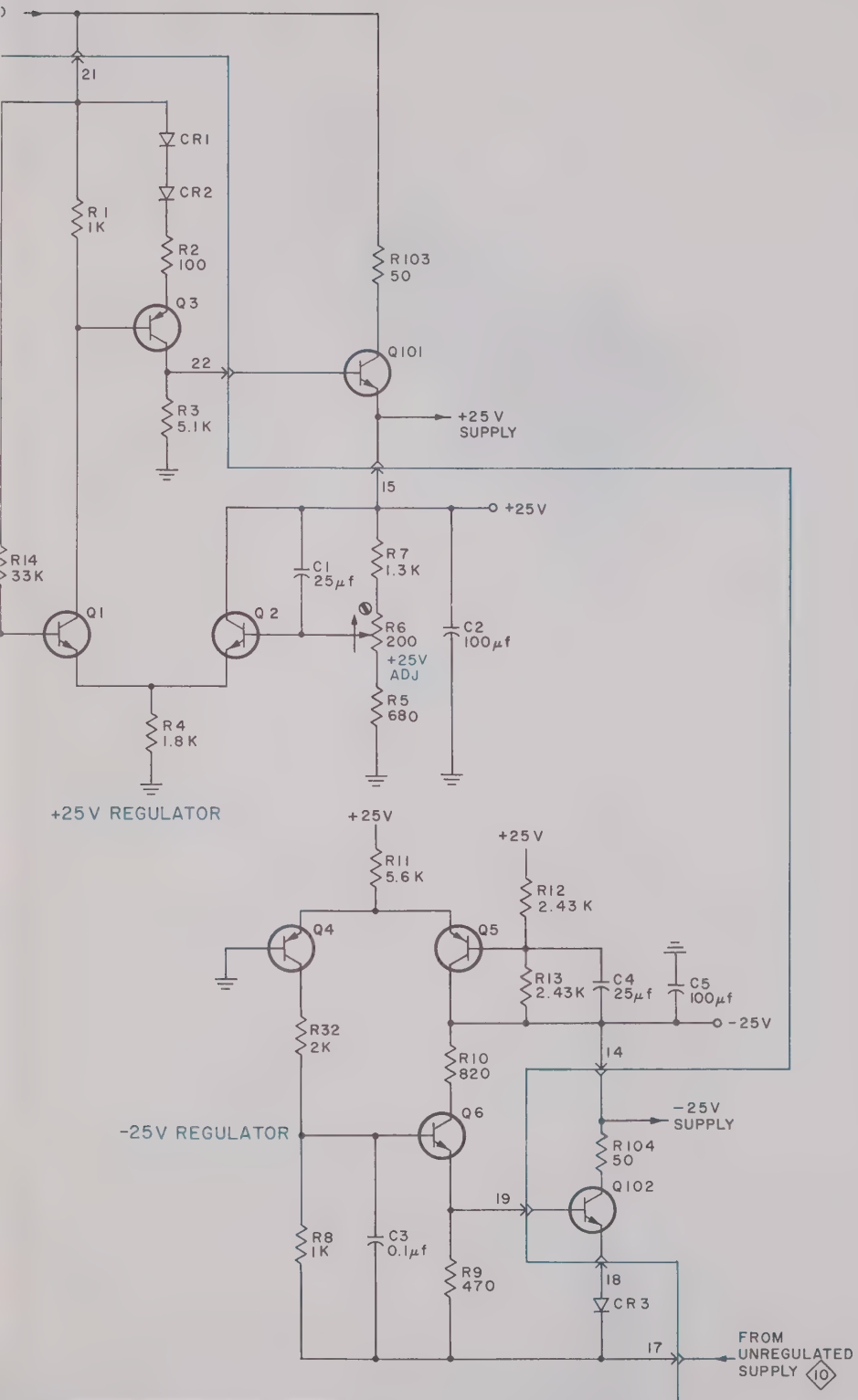


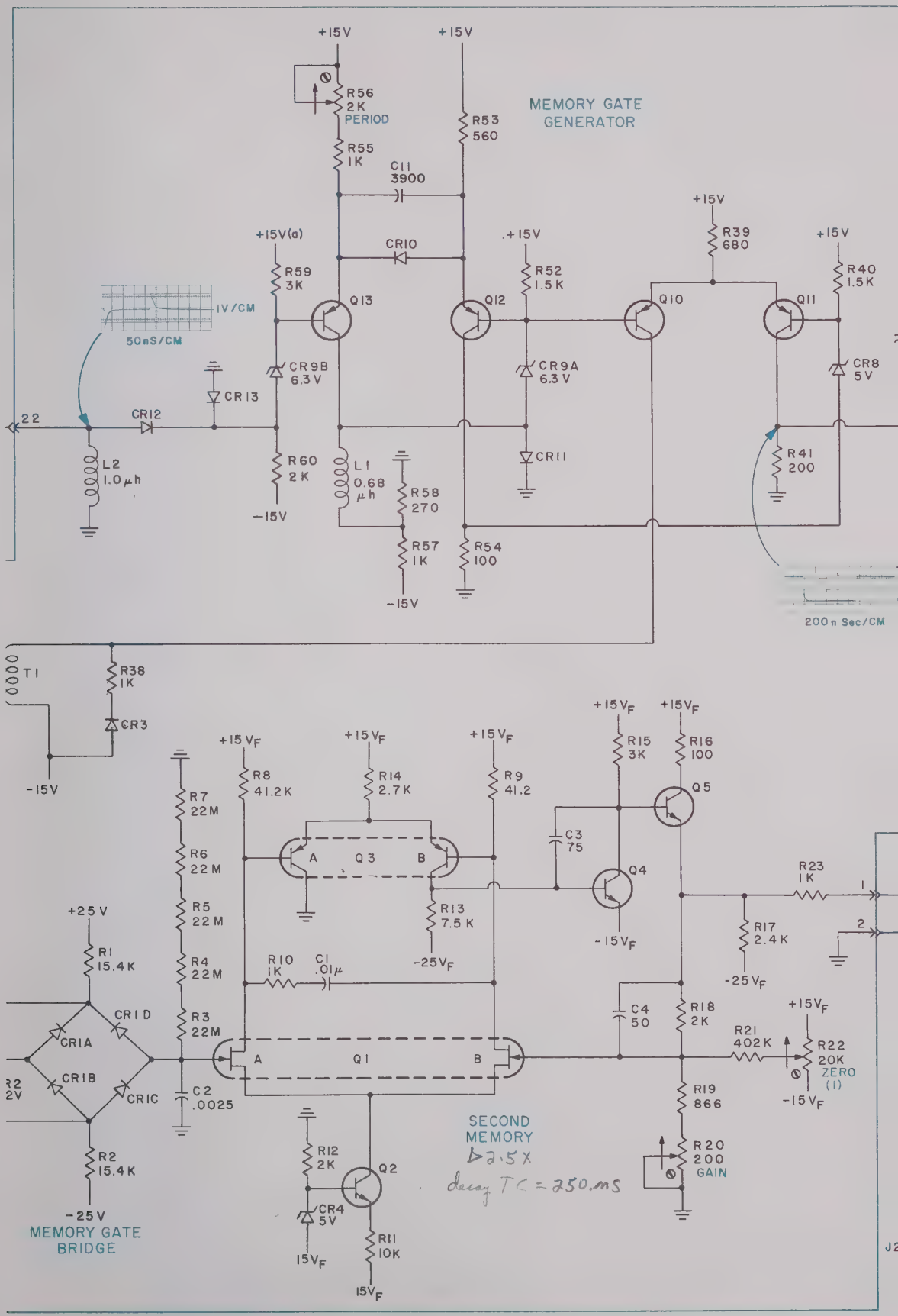
Fig. 6-7 Counter Board 12643

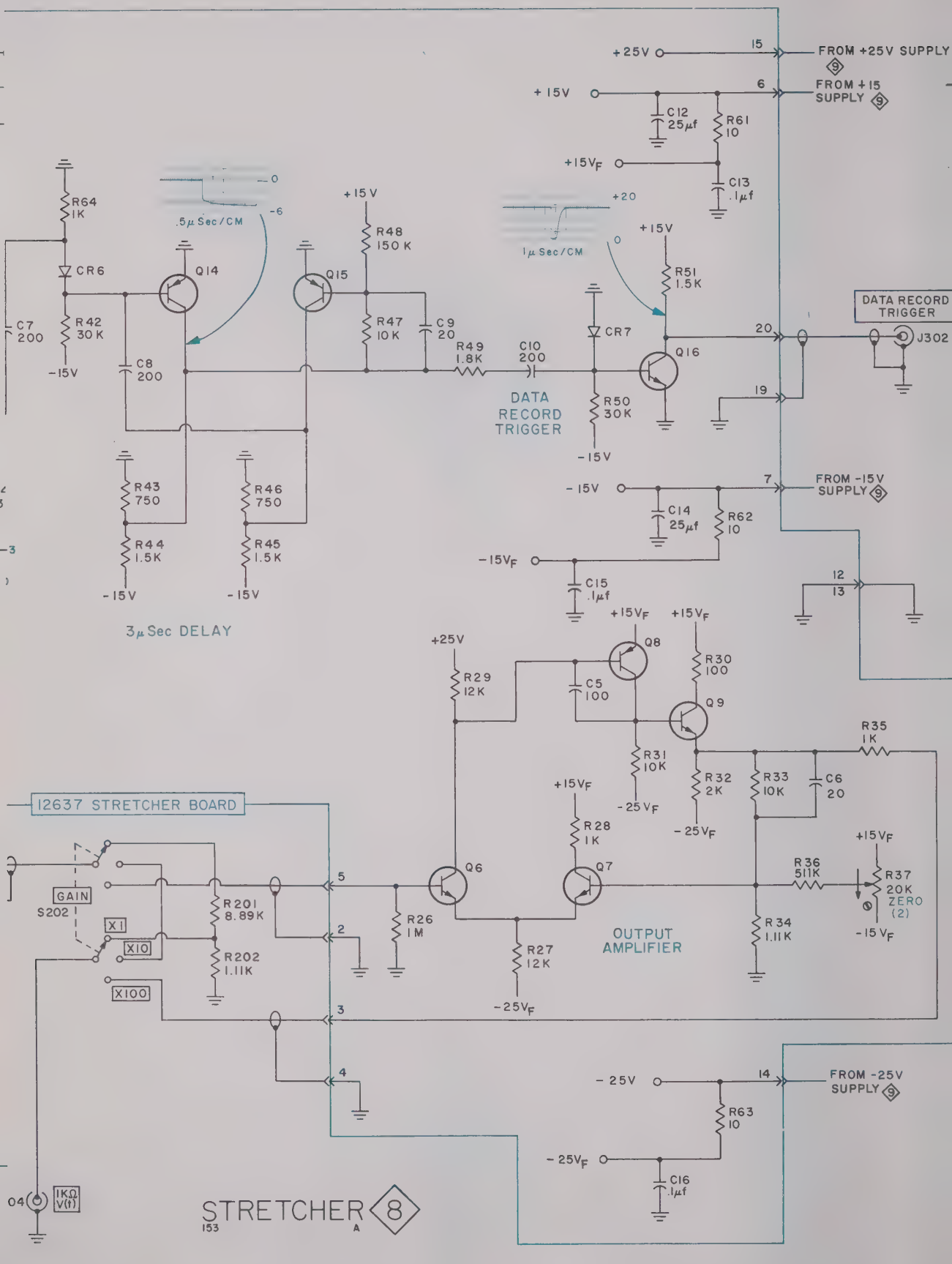

R110
270K
DS
210
1
2
3
4
B101
FAN
T101
S201
POWER
F301
1A FAST
F302
1A FAST
J301
117 VAC
50/60 Hz
234 OPTION
DS 201
R110
100K
1 BLK/RED
2 BLK/GRN
3 BLK/YEL
4 BLK
B101
FAN
S201
POWER
F301
1A FAST
F302
1A FAST
J301
117 VAC
50/60 Hz
T101

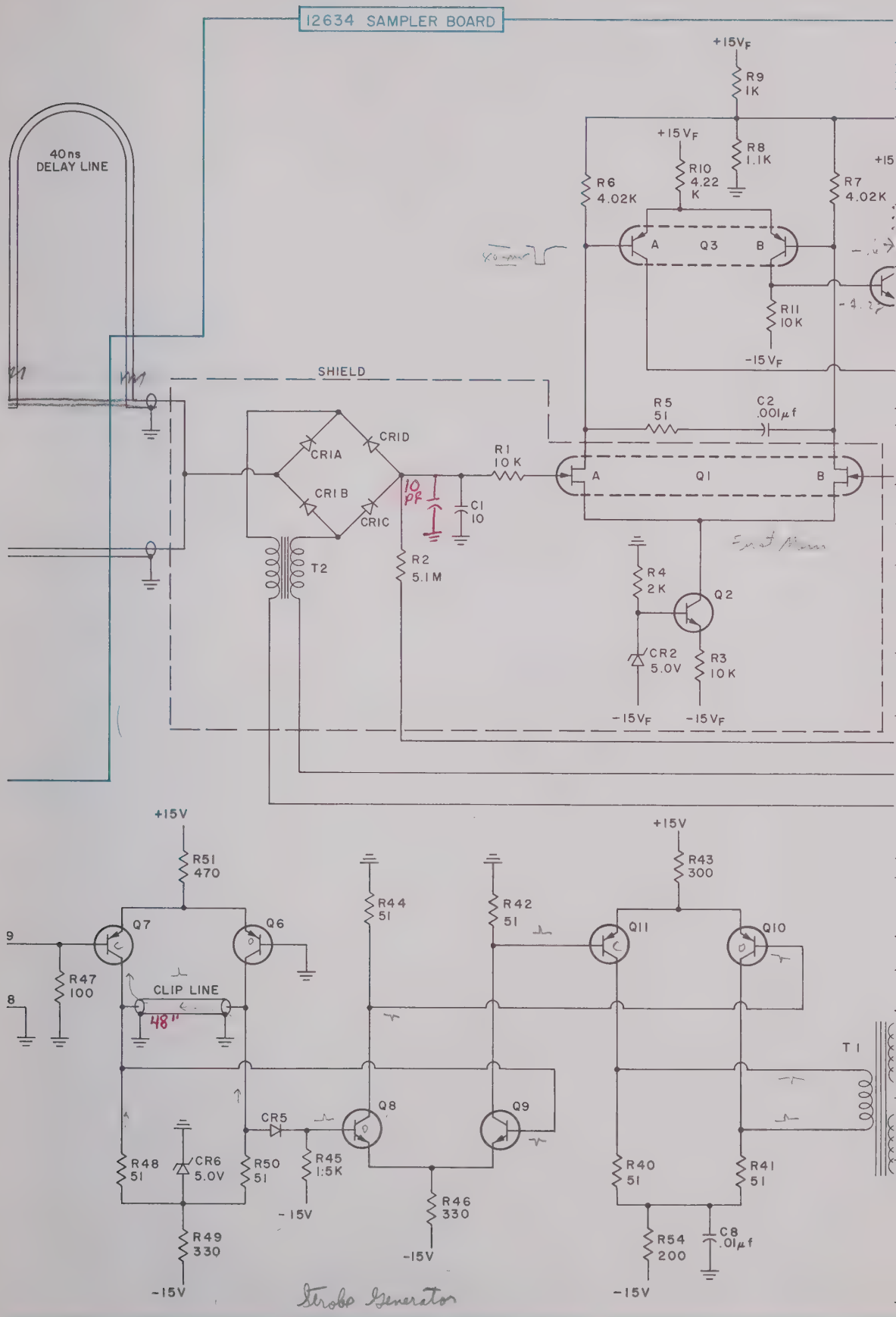

CR101
R101
2.7
TO R103 AND
PIN 21 REGULATOR BOARD 9
CR102
C101
1500μf
CR103
C102
1500μf
CR104
R102
2.7
TO REGULATOR BOARD
PIN 17 9
CR109
R109
1
CR111
CR110
C107
4000μf
CR112
Q105
+15V
+3.6V REGULATOR
R30
750
+15V
2
R29
510
Q13
CR6
4.3V
+3.6V
1
+3.6V
SUPPLY
C11
100μf
R31
62
12649 REGULATOR
BOARD CONT'D 9
CR105
R105
1
TO R107 AND
REGULATOR BOARD
PIN 4 9
CR106
C103
1500μf
C104
1500μf
CR107
C105
1500μf
C106
1500μf
CR108
R106
1
TO R108 AND
REGULATOR BOARD
PIN 8 9

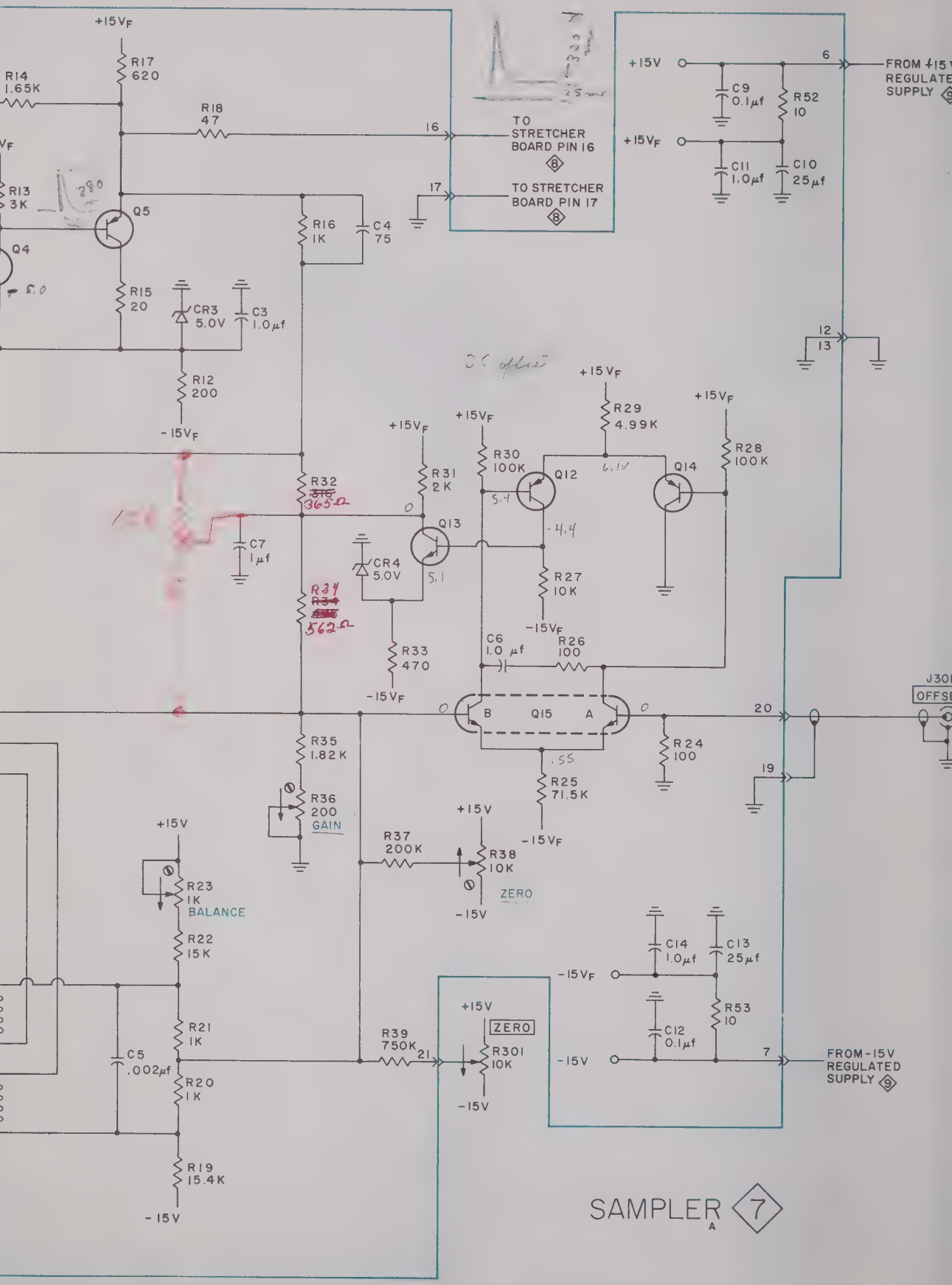

FROM UNREGULATED SUPPLY 10
FROM UNREGULATED SUPPLY 10
4
R107 3
Q103
3
R17 200
R16 1K
Q9
+15 V SUPPLY
12649 REGULATOR BOARD CONT'D 10
6
+15V
R21 470
C6 25μf
R15 680
CR4
C7 100μf
R20 200
+15V ADJ
Q8
Q7
CR5 9.0V
R19 750
R18 1.3 K
+15 V REGULATOR
+15 V
R22 2.7K
+15 V
R28 1K
Q11
Q10
C10 100μf
C9 25μf
R27 1K
7
-15 V SUPPLY
Q104
10
R26 1.5 K
C8 1μf
R23 1.5 K
-15V REGULATOR
Q12
R108 10
R25 120
R24 3K
FROM UNREGULATED SUPPLY 10
8
-25 V

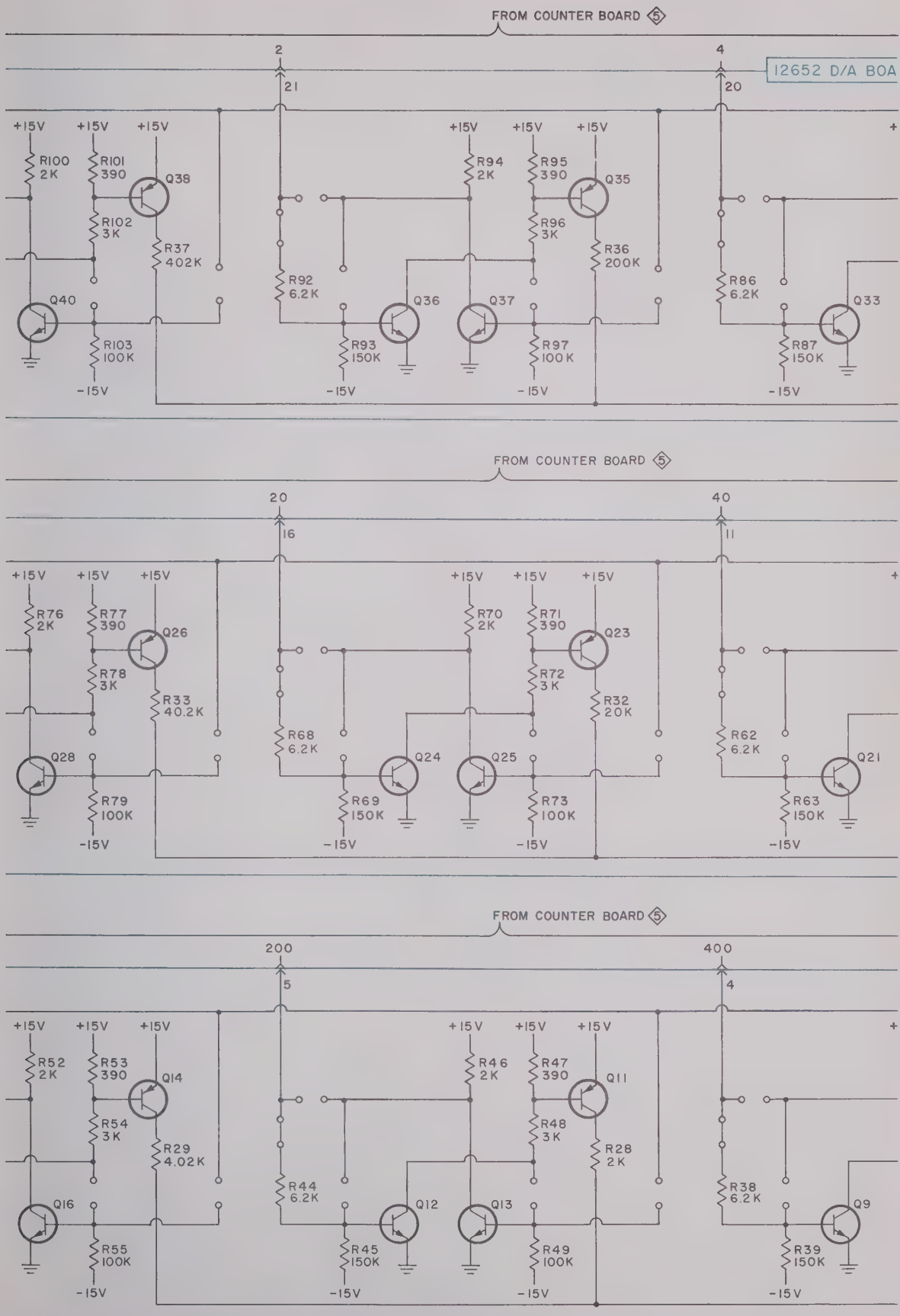

21
CR1
CR2
R1
1K
R2
100
Q3
R103
50
Q101
22
R3
5.1K
+25 V
SUPPLY
15
+25V
R14
33K
C1
25μf
R7
1.3K
Q1
Q2
R6
200
+25V
ADJ
C2
100μf
R5
680
R4
1.8K
+25V REGULATOR
+25V
R11
5.6K
+25V
R12
2.43 K
Q4
Q5
R13
2.43K
C4
25μf
C5
100μf
-25V
R32
2K
R10
820
14
-25V
SUPPLY
-25V REGULATOR
Q6
R104
50
Q102
19
R8
1K
C3
0.1μf
R9
470
18
CR3
17
FROM
UNREGULATED
SUPPLY
10

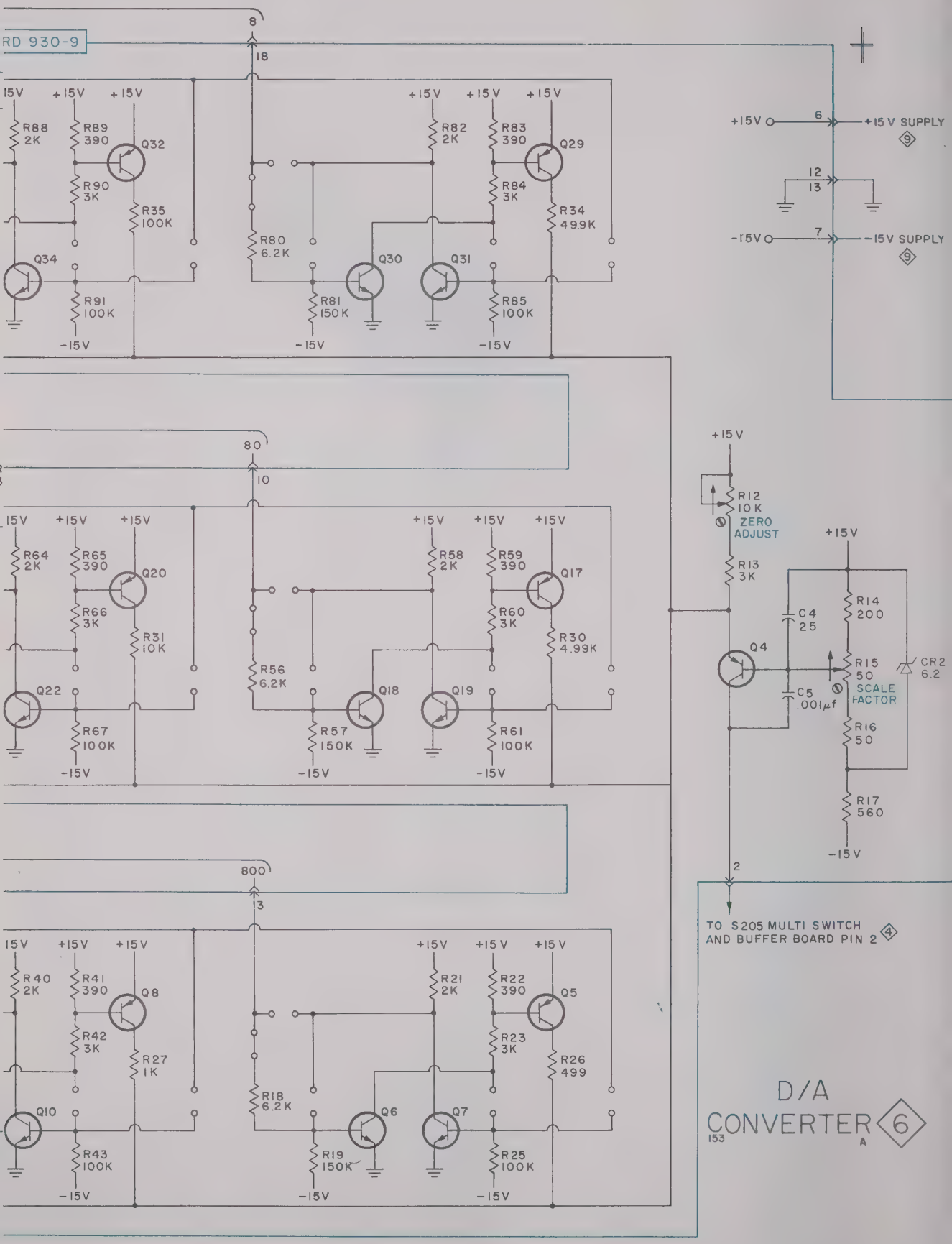

MEMORY GATE GENERATOR
+15V
R56 2K PERIOD
R55 1K
C11 3900
R53 560
+15V(a)
R59 3K
CR10
Q13
Q12
R52 1.5K
Q10
R39 680
Q11
R40 1.5K
CR8 5V
1V/CM
50nS/CM
CR9B 6.3V
CR13
CR12
CR9A 6.3V
CR11
L2 1.0μh
R60 2K
L1 0.68μh
R58 270
R57 1K
R54 100
R41 200
200n Sec/CM
T1
R38 1K
CR3
-15V
+15V_F
R8 41.2K
R14 2.7K
R9 41.2
R15 3K
R16 100
Q5
C3 75
Q4
R23 1K
R7 22M
R6 22M
R5 22M
R4 22M
R3 22M
Q3
A
B
R13 7.5K
-25V_F
R17 2.4K
+25 V
R1 15.4K
R10 1K
C1 .01μ
CR1D
CR1A
CR1B
CR1C
Q1
C4 50
R18 2K
R21 402K
R22 20K ZERO (1)
C2 .0025
R19 866
R20 200 GAIN
SECOND MEMORY
▷2.5X
decay TC = 250.ms
R12 2K
Q2
CR4 5V
R11 10K
R2 15.4K
-25 V
MEMORY GATE BRIDGE

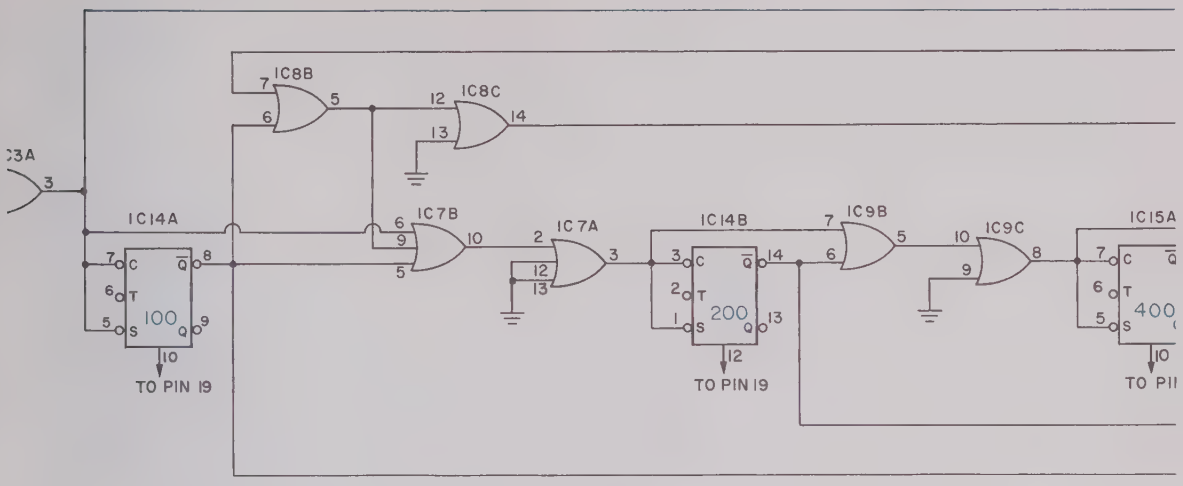

+25V
15
FROM +25V SUPPLY
9
+15V
6
FROM +15 SUPPLY
9
C12 25μf
R61 10
+15VF
C13 .1μf
R64 1K
CR6
Q14
Q15
R48 150 K
R47 10K
C9 20
R49 1.8K
C10 200
CR7
Q16
R51 1.5K
R50 30K
C7 200
R42 30K
-15V
C8 200
.5μ Sec/CM
1μ Sec/CM
+20
0
-6
DATA RECORD TRIGGER
J302
20
19
DATA RECORD TRIGGER
R43 750
R44 1.5K
R46 750
R45 1.5K
3μ Sec DELAY
-15V
7
FROM -15V SUPPLY
9
C14 25μf
R62 10
-15VF
C15 .1μf
12
13
+15VF
Q8
Q9
R30 100
+25V
R29 12K
C5 100
R31 10K
R35 1K
R32 2K
R33 10K
C6 20
-25VF
12637 STRETCHER BOARD
R28 1K
Q6
Q7
R36 511K
R37 20K ZERO (2)
GAIN
S202
X1
X10
X100
R201 8.89K
R202 1.11K
R26 1M
R27 12K
R34 1.11K
OUTPUT AMPLIFIER
5
2
3
4
- 25V
14
FROM -25V SUPPLY
9
R63 10
C16 .1μf
04
1KΩ V(f)
STRETCHER 8
153
A

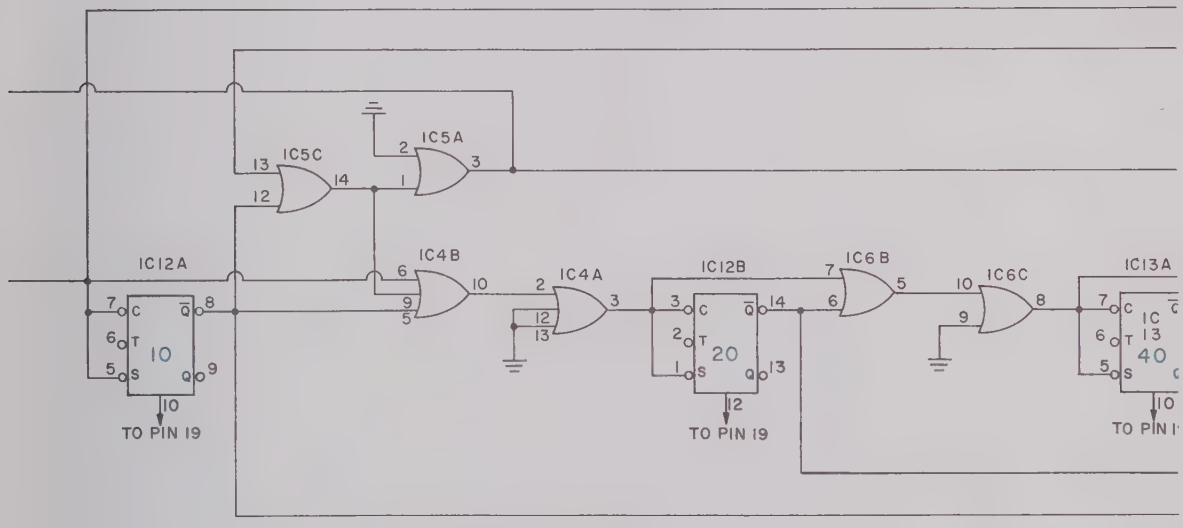

12634 SAMPLER BOARD
40ns DELAY LINE
SHIELD
+15V$_F$
R9 1K
R8 1.1K
R10 4.22 K
R6 4.02K
R7 4.02K
Q3
R11 10K
-15V$_F$
R5 51
C2 .001μf
CR1A
CR1B
CR1C
CR1D
10 PF
C1 10
R1 10K
Q1
T2
R2 5.1M
R4 2K
Q2
CR2 5.0V
R3 10K
+15V
R51 470
Q7
Q6
R47 100
CLIP LINE
48"
R44 51
R42 51
R43 300
Q11
Q10
T1
CR5
Q8
Q9
R48 51
CR6 5.0V
R50 51
R45 1.5K
R46 330
R49 330
R40 51
R41 51
R54 200
C8 .01μf
-15V
Strobe Generator

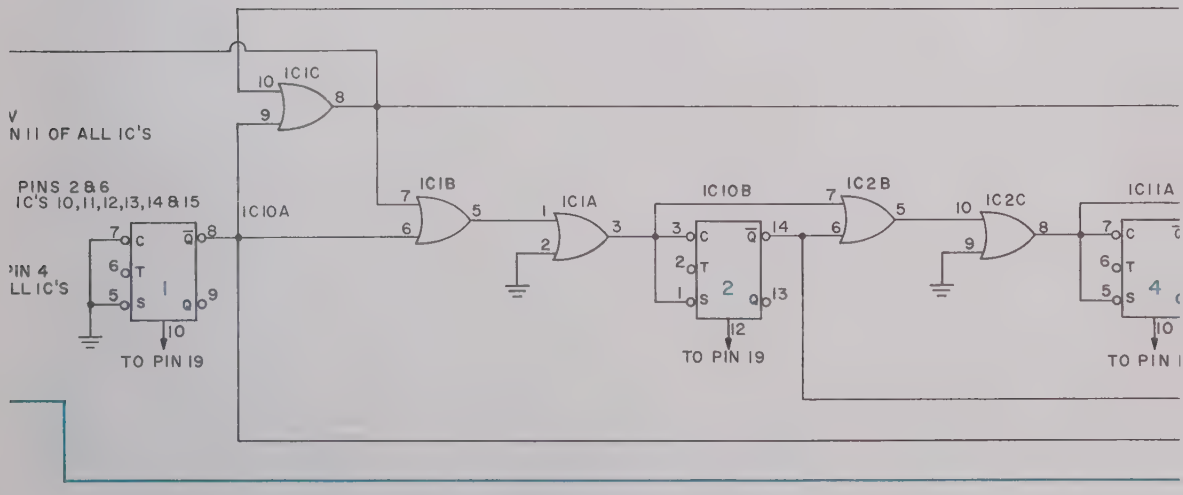

+15VF
R17 620
R14 1.65K
R18 47
16
TO STRETCHER BOARD PIN 16
8
17
TO STRETCHER BOARD PIN 17
8
+15V
C9 0.1μf
R52 10
6
FROM +15V REGULATED SUPPLY
9
+15VF
C11 1.0μf
C10 25μf
R13 3K
Q5
Q4
R16 1K
C4 75
R15 20
CR3 5.0V
C3 1.0μf
R12 200
-15VF
12
13
+15VF
R29 4.99K
+15VF
+15VF
R30 100K
Q12
Q14
R28 100K
R31 2K
R32 365Ω
Q13
CR4 5.0V
C7 1μf
R27 10K
-15VF
R34 562Ω
R33 470
-15VF
C6 1.0 μf
R26 100
B
Q15
A
20
R24 100
J30
OFFSE
R35 1.82K
R36 200 GAIN
R25 71.5K
-15VF
19
+15V
R37 200K
+15V
R38 10K ZERO
-15V
+15V
R23 1K BALANCE
R22 15K
C14 1.0μf
C13 25μf
-15VF
R53 10
C12 0.1μf
-15V
7
FROM -15V REGULATED SUPPLY
9
R21 1K
C5 .002μf
R20 1K
R39 750K
21
+15V
ZERO
R301 10K
-15V
R19 15.4K
-15V
SAMPLER A 7

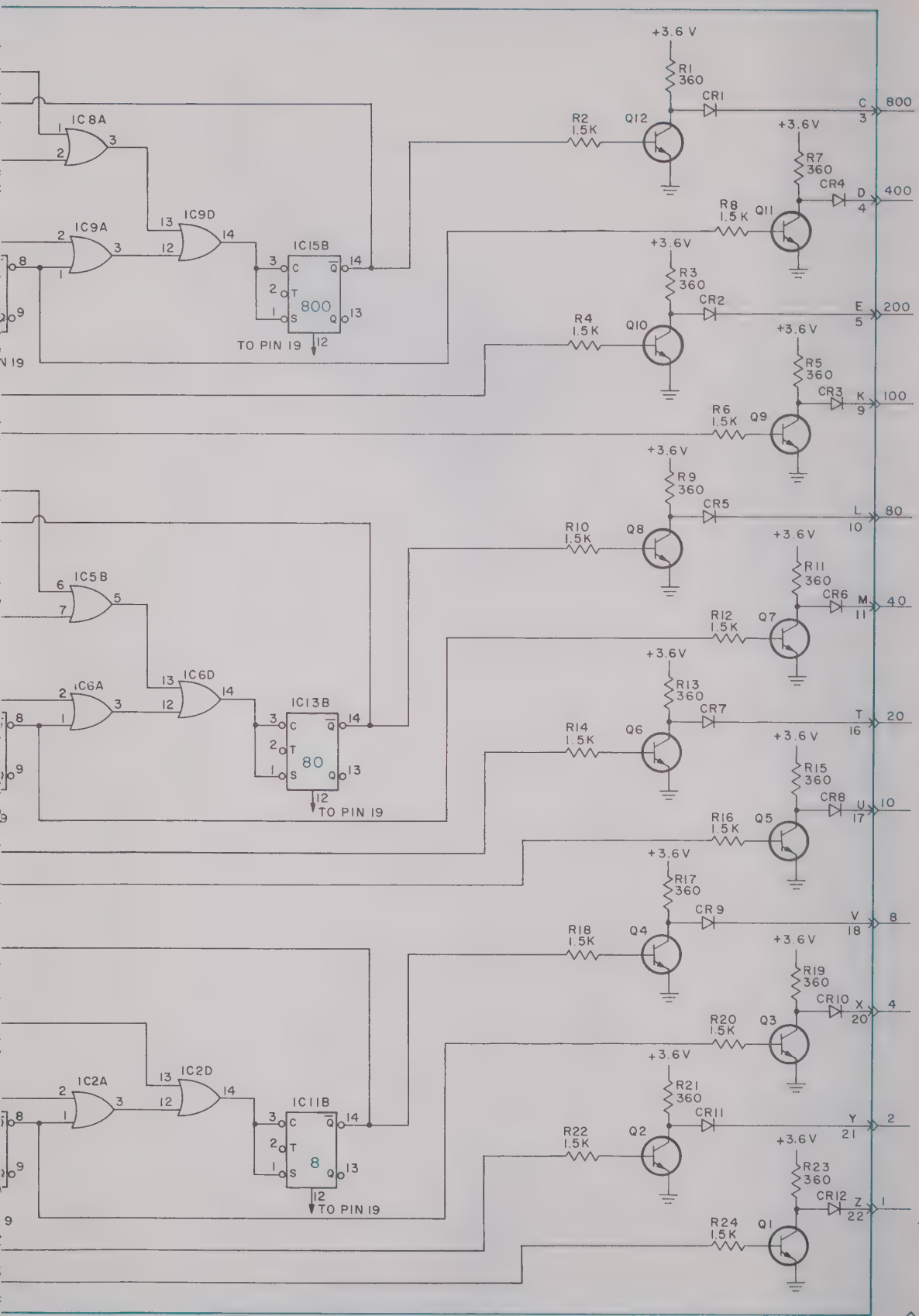

FROM COUNTER BOARD 5
12652 D/A BOA
2
21
4
20
+15V
R100 2K
R101 390
Q38
R102 3K
R37 402K
Q40
R103 100K
-15V
R92 6.2K
Q36
R93 150K
R94 2K
R95 390
Q35
R96 3K
R36 200K
Q37
R97 100K
R86 6.2K
Q33
R87 150K
FROM COUNTER BOARD 5
20
16
40
11
R76 2K
R77 390
Q26
R78 3K
R33 40.2K
Q28
R79 100K
R68 6.2K
Q24
R69 150K
R70 2K
R71 390
Q23
R72 3K
R32 20K
Q25
R73 100K
R62 6.2K
Q21
R63 150K
FROM COUNTER BOARD 5
200
5
400
4
R52 2K
R53 390
Q14
R54 3K
R29 4.02K
Q16
R55 100K
R44 6.2K
Q12
R45 150K
R46 2K
R47 390
Q11
R48 3K
R28 2K
Q13
R49 100K
R38 6.2K
Q9
R39 150K

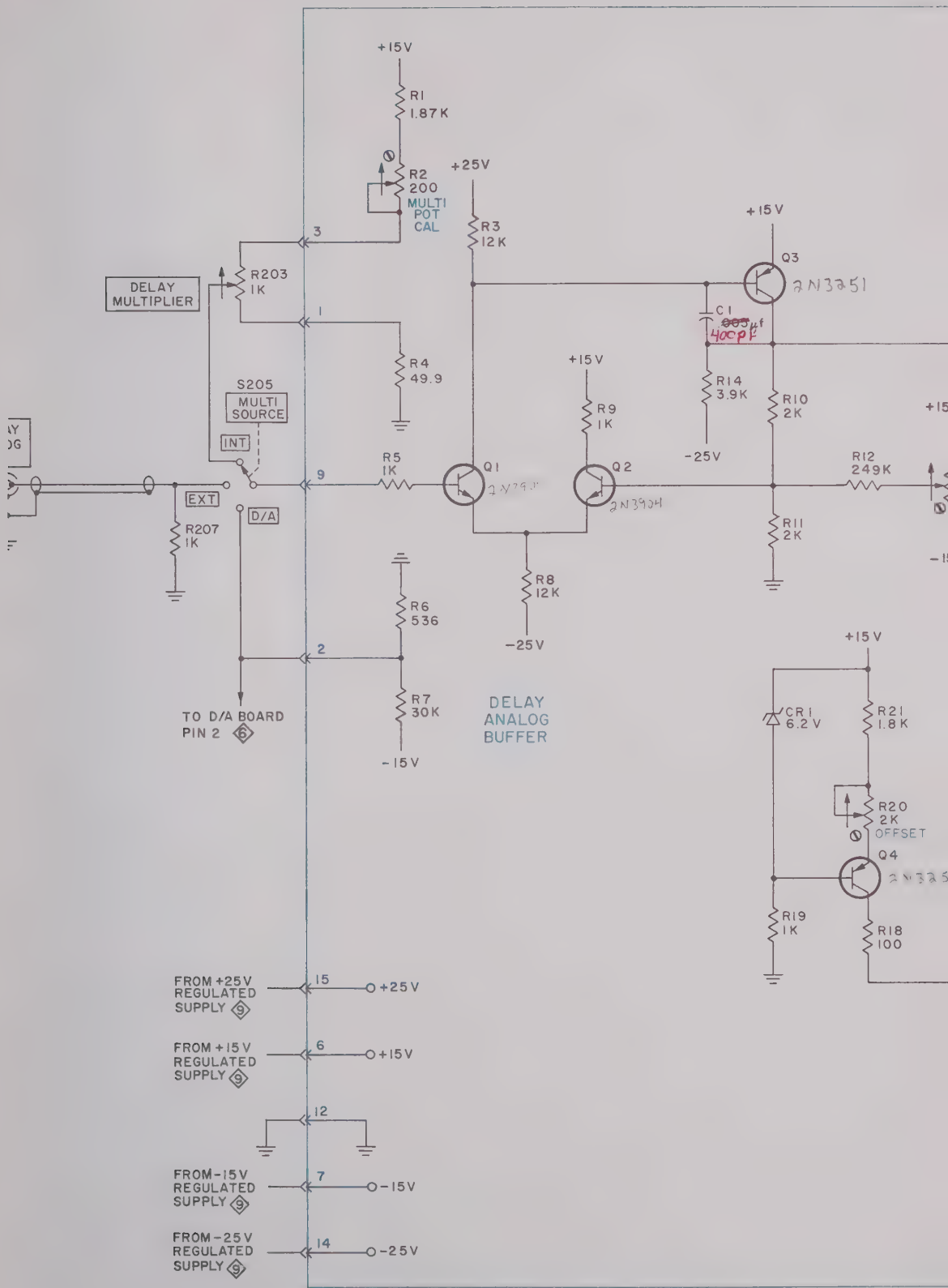

RD 930-9
8
18
+15V
+15V SUPPLY
9
12
13
-15V
-15V SUPPLY
9
R88 2K
R89 390
Q32
R90 3K
R35 100K
Q34
R91 100K
-15V
R80 6.2K
Q30
R81 150K
R82 2K
R83 390
Q29
R84 3K
R34 49.9K
Q31
R85 100K
80
10
R64 2K
R65 390
Q20
R66 3K
R31 10K
Q22
R67 100K
R56 6.2K
Q18
R57 150K
R58 2K
R59 390
Q17
R60 3K
R30 4.99K
Q19
R61 100K
R12 10K
ZERO ADJUST
R13 3K
C4 25
Q4
C5 .001μf
R14 200
R15 50
SCALE FACTOR
CR2 6.2
R16 50
R17 560
2
TO S205 MULTI SWITCH AND BUFFER BOARD PIN 2
4
800
3
R40 2K
R41 390
Q8
R42 3K
R27 1K
Q10
R43 100K
R18 6.2K
Q6
R19 150K
R21 2K
R22 390
Q5
R23 3K
R26 499
Q7
R25 100K
D/A CONVERTER
153
A
6

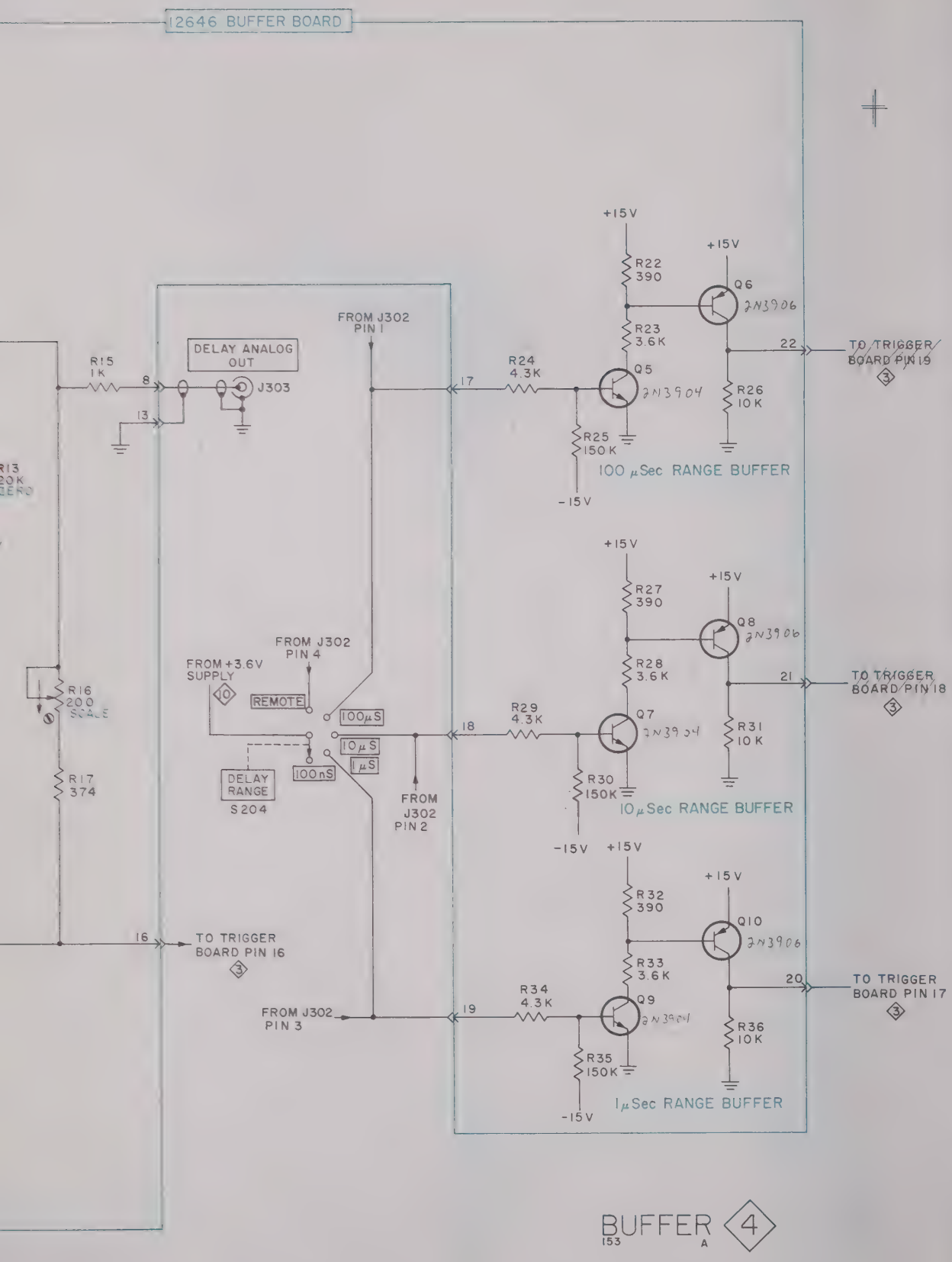

IC8B
IC8C
IC14A
IC7B
IC7A
IC14B
IC9B
IC9C
IC15A
100
200
400
TO PIN 19
TO PIN 19

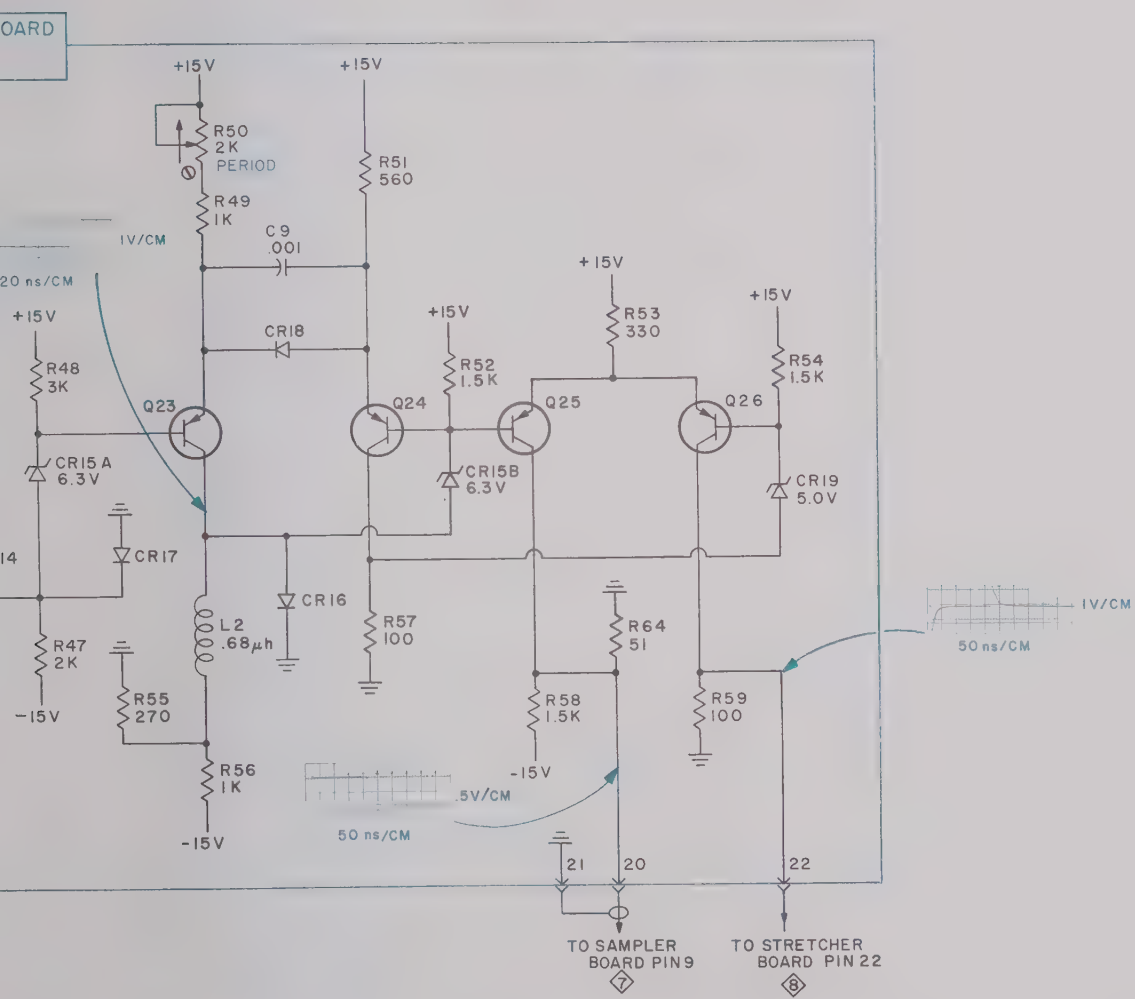

IC5C
IC5A
IC12A
IC4B
IC4A
IC12B
IC6B
IC6C
IC13A
10
20
40
TO PIN 19
TO PIN 19


IC1C
OF ALL IC'S
PINS 2 & 6
IC'S 10,11,12,13,14 & 15
IC10A
IC1B
IC1A
IC10B
IC2B
IC2C
IC11A
1
2
4
TO PIN 19
TO PIN 19

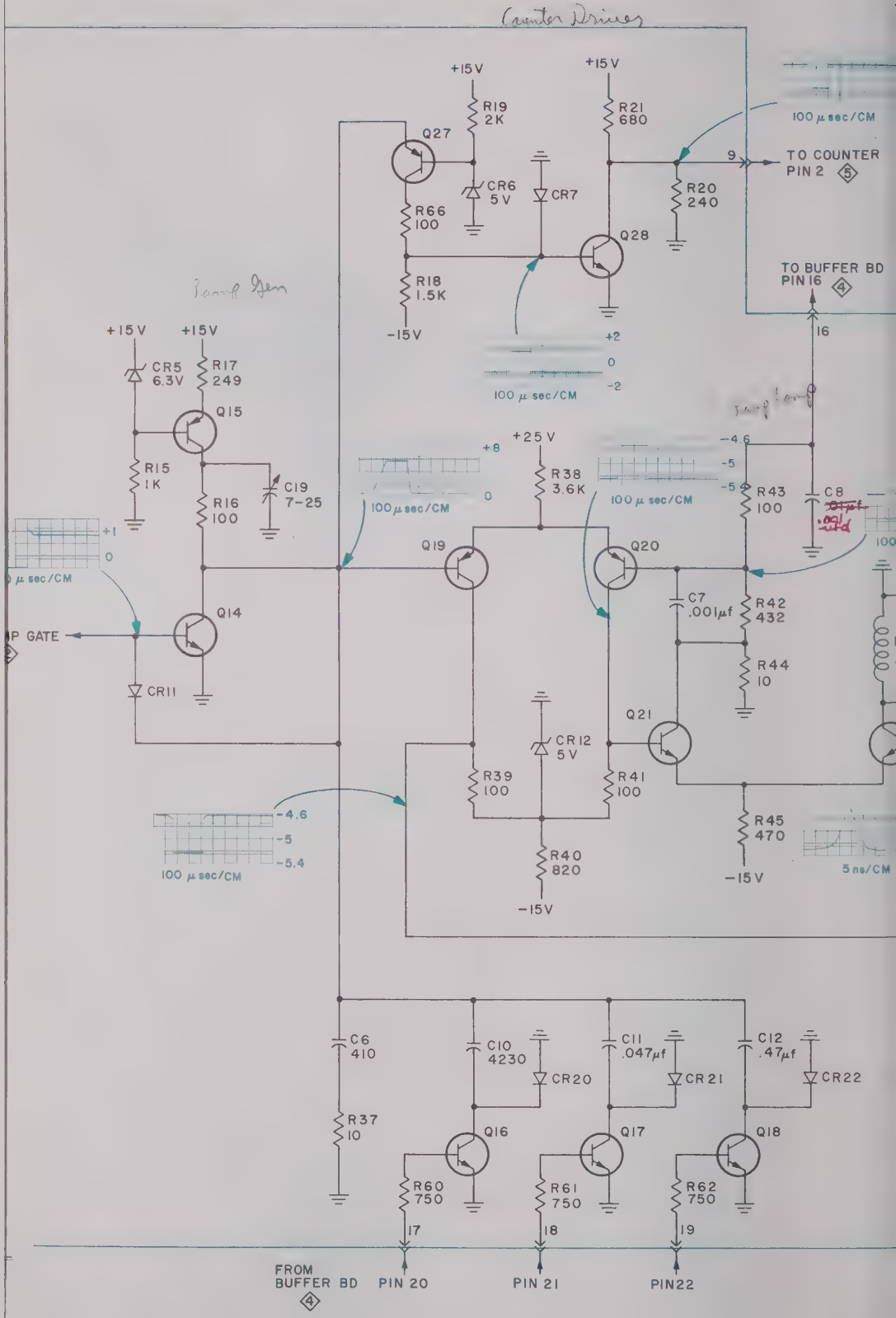

+3.6 V
R1 360
CR1
R2 1.5K
Q12
C 3 800
IC8A
IC9A
IC9D
IC15B
800
TO PIN 19
R7 360
CR4
R8 1.5 K
Q11
D 4 400
R3 360
CR2
R4 1.5K
Q10
E 5 200
R5 360
CR3
R6 1.5K
Q9
K 9 100
R9 360
CR5
R10 1.5K
Q8
L 10 80
IC5B
IC6A
IC6D
IC13B
80
R11 360
CR6
R12 1.5K
Q7
M 11 40
R13 360
CR7
R14 1.5K
Q6
T 16 20
R15 360
CR8
R16 1.5K
Q5
U 17 10
R17 360
CR9
R18 1.5K
Q4
V 18 8
R19 360
CR10
R20 1.5K
Q3
X 20 4
IC2A
IC2D
IC11B
8
R21 360
CR11
R22 1.5K
Q2
Y 21 2
R23 360
CR12
R24 1.5K
Q1
Z 22 1
TO PIN 19
TO D/A BOA
6


+15V
R1
1.87K
R2
200
MULTI
POT
CAL
+25V
R3
12K
3
DELAY
MULTIPLIER
R203
1K
1
R4
49.9
S205
MULTI
SOURCE
INT
EXT
D/A
9
R5
1K
Q1
2N3904
Q2
2N3904
R8
12K
-25V
R6
536
2
R7
30K
-15V
TO D/A BOARD
PIN 2
6
DELAY
ANALOG
BUFFER
+15V
Q3
2N3251
C1
400pf
R14
3.9K
R10
2K
-25V
R12
249K
R11
2K
+15V
R9
1K
CR1
6.2V
R21
1.8K
R20
2K
OFFSET
Q4
R19
1K
R18
100
FROM +25V
REGULATED
SUPPLY
9
15
+25V
FROM +15V
REGULATED
SUPPLY
9
6
+15V
12
FROM -15V
REGULATED
SUPPLY
9
7
-15V
FROM -25V
REGULATED
SUPPLY
9
14
-25V


12646 BUFFER BOARD
+15V
R22
390
Q6
2N3906
R23
3.6K
22
TO TRIGGER BOARD PIN 19
3
DELAY ANALOG OUT
R15
1K
8
J303
13
FROM J302 PIN 1
R24
4.3K
17
Q5
2N3904
R26
10K
R25
150K
-15V
100 μSec RANGE BUFFER
R27
390
Q8
2N3906
R28
3.6K
21
TO TRIGGER BOARD PIN 18
FROM J302 PIN 4
FROM +3.6V SUPPLY
10
REMOTE
100μS
10μS
1μS
100nS
DELAY RANGE
S204
R29
4.3K
18
Q7
2N3904
R31
10K
R30
150K
FROM J302 PIN 2
10 μSec RANGE BUFFER
R16
200
SCALE
R17
374
16
TO TRIGGER BOARD PIN 16
R32
390
Q10
2N3906
R33
3.6K
20
TO TRIGGER BOARD PIN 17
FROM J302 PIN 3
R34
4.3K
19
Q9
2N3904
R36
10K
R35
150K
1μSec RANGE BUFFER
BUFFER 4
153 A



DELAY GENERATOR 153 A 3


Counter Drivers
+15V
R19 2K
Q27
CR6 5V
R66 100
R18 1.5K
-15V
+15V
R21 680
CR7
Q28
R20 240
9
TO COUNTER PIN 2
5
100 μ sec/CM
TO BUFFER BD PIN 16
4
16
+2
0
-2
100 μ sec/CM
+15V
+15V
CR5 6.3V
R17 249
Q15
R15 1K
R16 100
C19 7-25
+1
0
μ sec/CM
P GATE
Q14
CR11
+8
0
100 μ sec/CM
+25 V
R38 3.6K
Q19
Q20
-4.6
-5
-5
100 μ sec/CM
R43 100
C8
C7 .001μf
R42 432
R44 10
Q21
CR12 5V
R39 100
R41 100
R40 820
-15V
R45 470
-15V
-4.6
-5
-5.4
100 μ sec/CM
5 ns/CM
C6 410
R37 10
C10 4230
CR20
C11 .047μf
CR21
C12 .47μf
CR22
Q16
Q17
Q18
R60 750
R61 750
R62 750
17
18
19
FROM BUFFER BD
4
PIN 20
PIN 21
PIN22